IC Packages, Connectors and Vias

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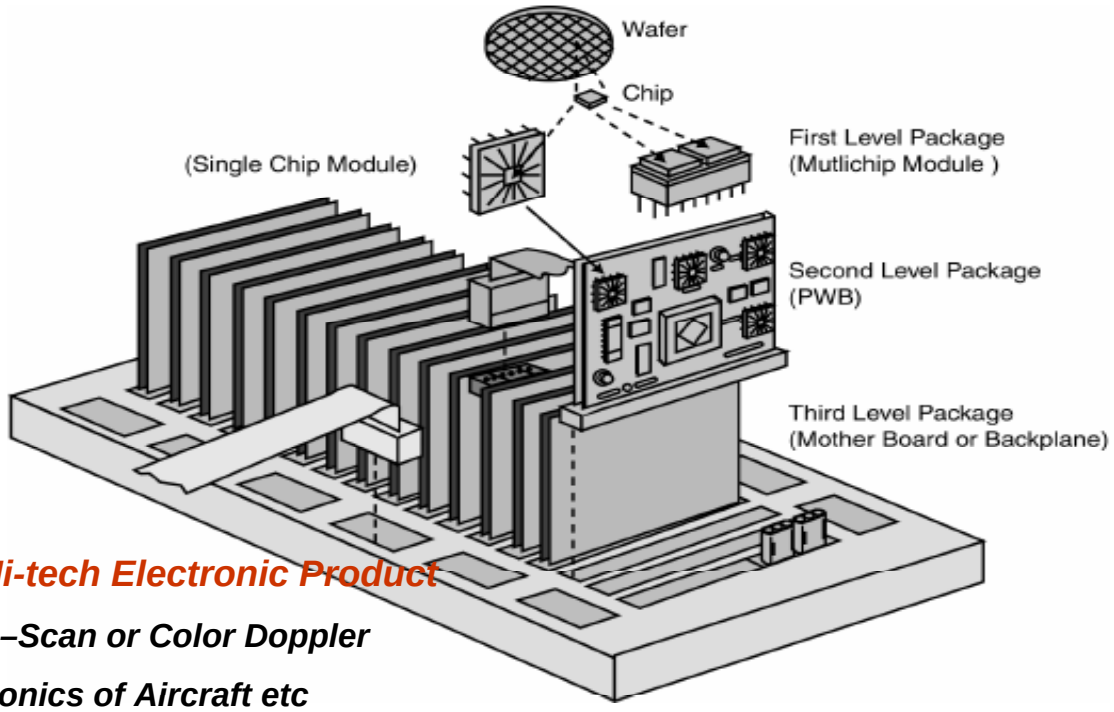
System Packaging Hierarchy



Any Hi-tech Electronic Product

- ***CT –Scan or Color Doppler***
- ***Avionics of Aircraft etc***

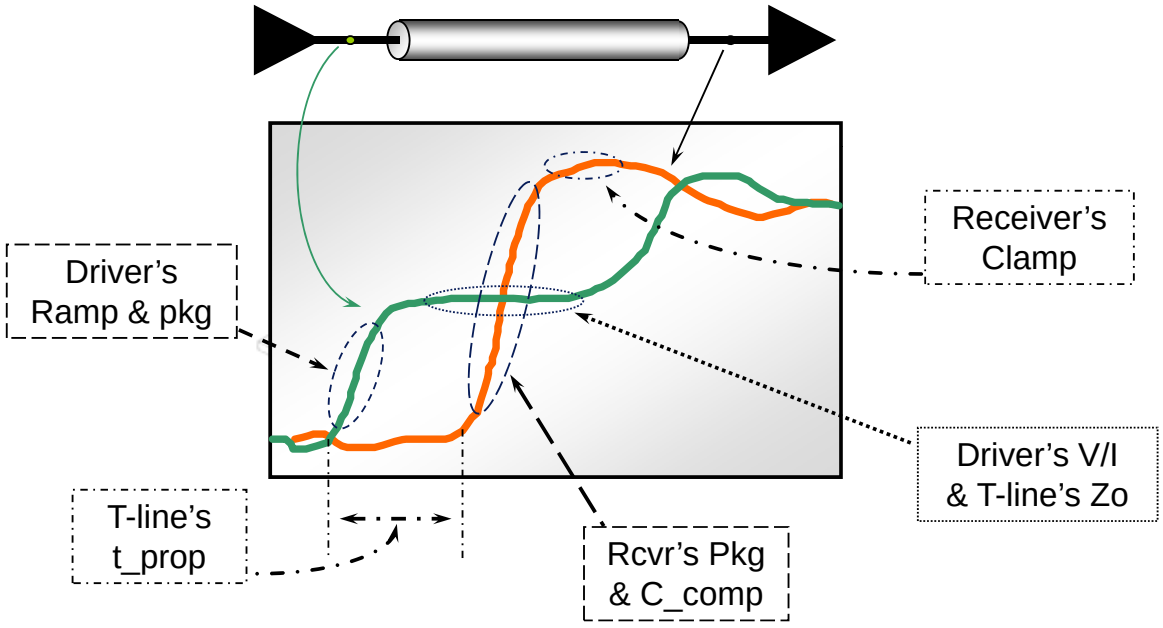
Today's Topics

- Why is packaging important ?
  - Trends in packaging
  - Impact on high speed signals
  - Package and connector models
  - IC packages
    - Through hole
    - Surface mount
  - Connectors
    - Surface mount
    - Through hole
- Via and Via Types
  - Via Modeling
  - Standard Sizes, HDI

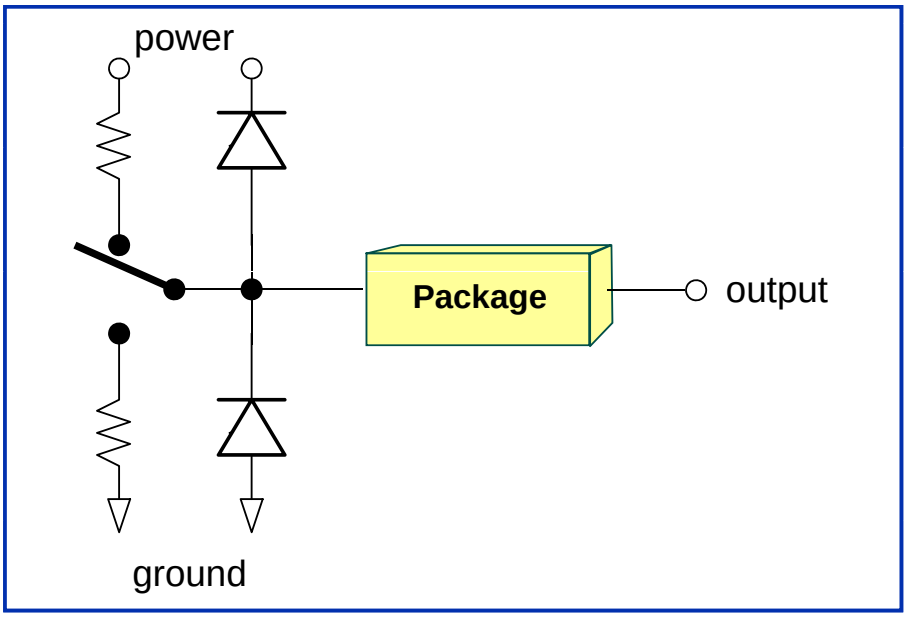
Package Selection

- In PCB Design we use prefabricated package.
- If multiple package are available, decide based upon
  - Temperature Rise (Commercial, Industrial, Military)
  - Mechanical Strength (Avionics, Industrial or home appliance)
  - Routability and Number of Layers
  - Rework and troubleshooting
  - Maximum CLK rate and Bus Speed
  - EMI and EMC requirement

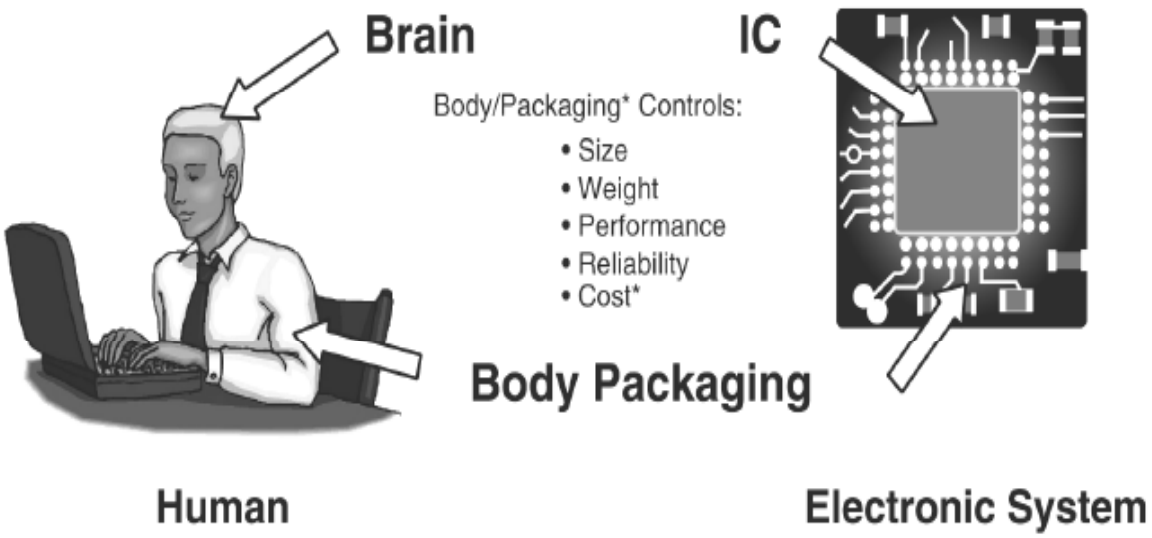
Impact of Packaging



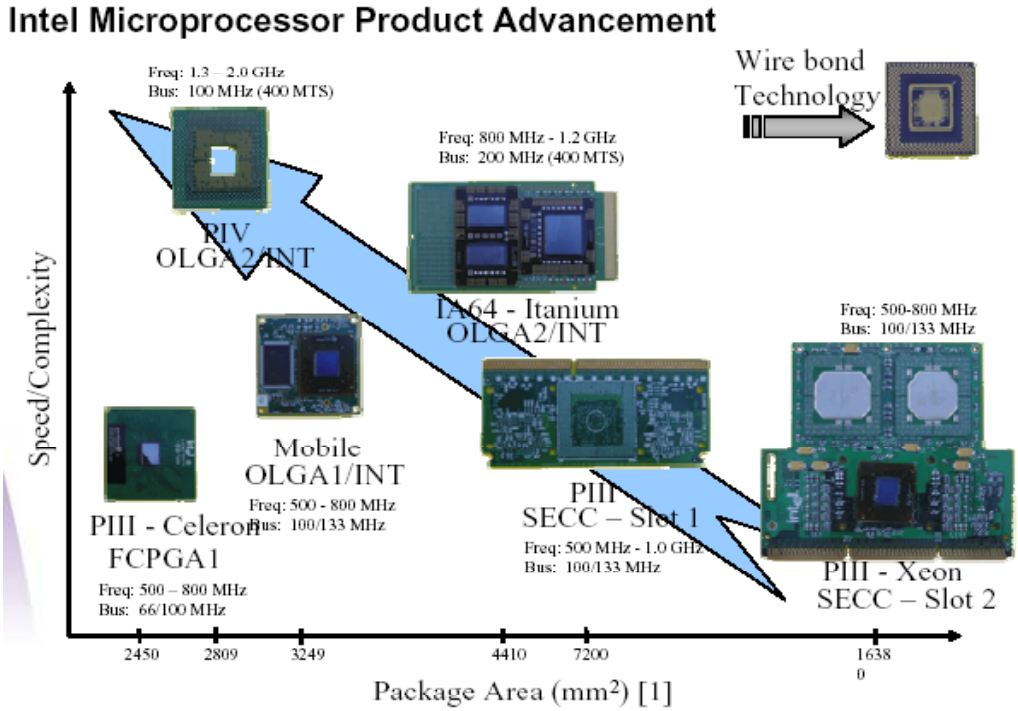
Physical Connection with outside world



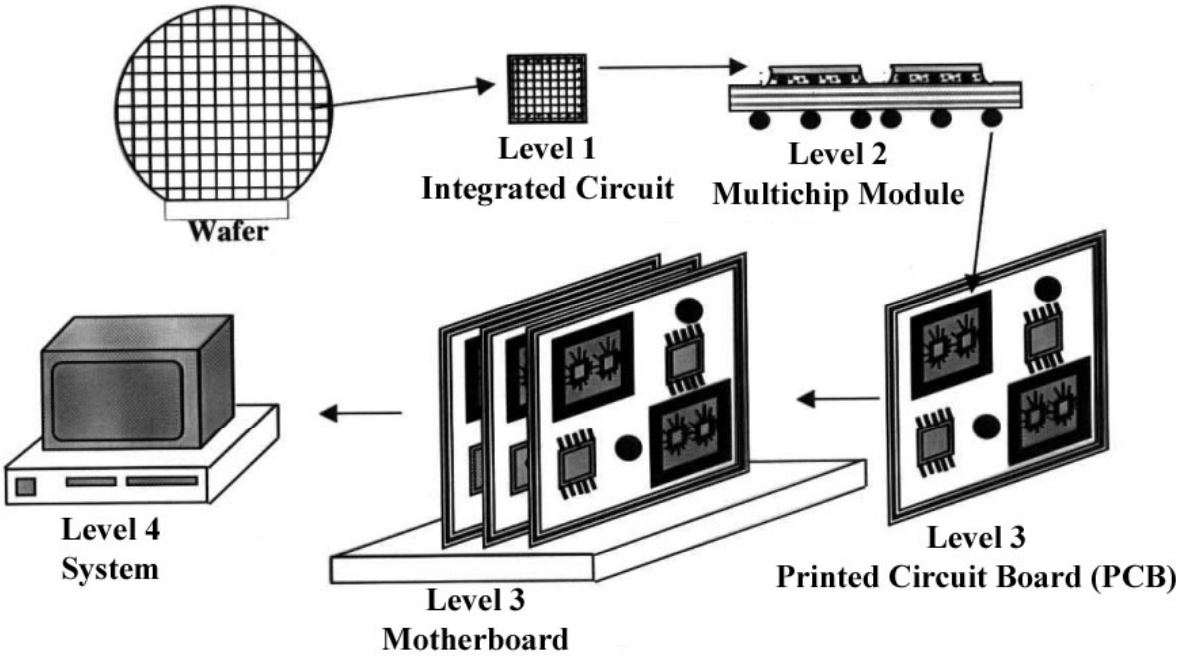
Analogy Between Human and Electronics



Trends in Packaging



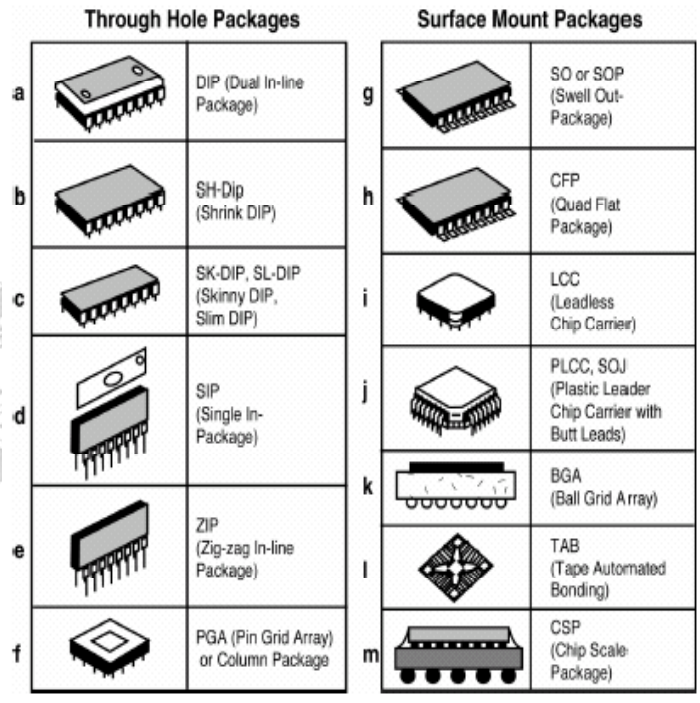
Levels of Packaging



Level 1:Single Chip Module (SCM)

SCM families:

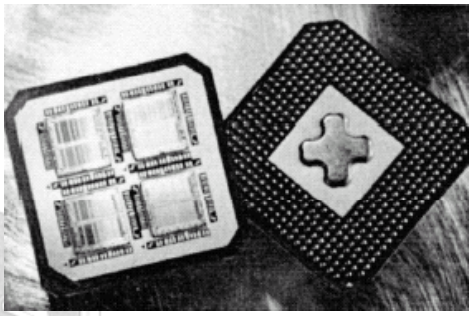
- **THP**
  - Single (SIP)
  - Dual (PDIP, CERDIP)
  - Area Array: Quad (PGA)
- **SMD**
  - Dual: Small outline (SOJ, SOP, TSOP)
  - Quad: Quad surface mount (PLCC, PQFP, CERQUAD)
  - Area Array: Grid array (PGA, BGA)



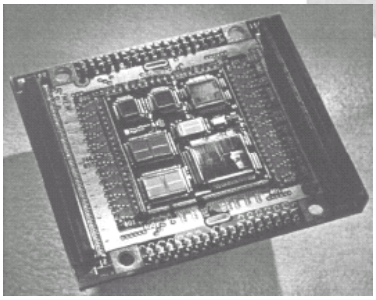
Level 2:Multi Chip Module (MCM)

- MCM-L
- MCM-C
- MCM-D
- MCM-S

MCM-L
486 Processor
Base of Similar
Material like PCB



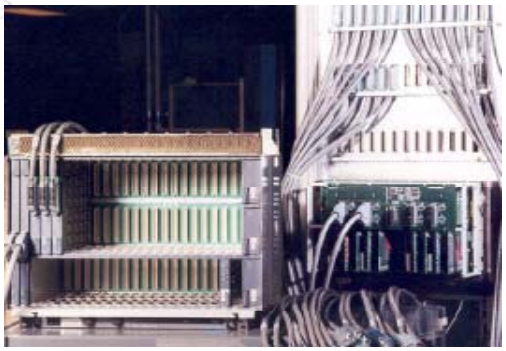
MCM-C
Motorola 88110 CPU
Ceramic Base



MCM-D
MMX Pentium on
Aluminum Base
covered by dielectric
Polymide

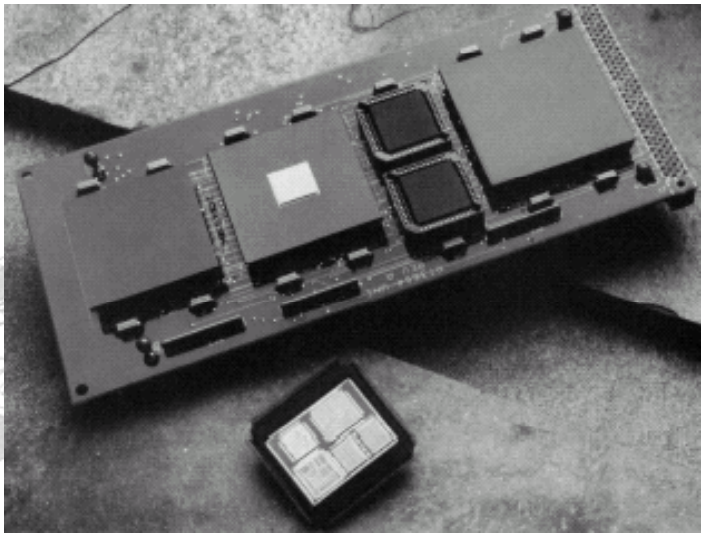
Level 3 &4 :PCB and Final Product

- Level-3: PCBs, PWBs and back planes
- Level-4 : Systems Level
  - Represents the final product/system and integration of PCBs
  - Subassemblies like power supplies
  - Items for user interface like CTR, Key Boards etc
  - Special components like fans and transformers
  - Wiring, cables and harnesses
  - Protective enclosure

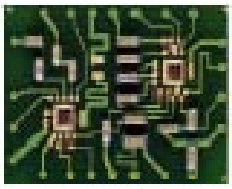


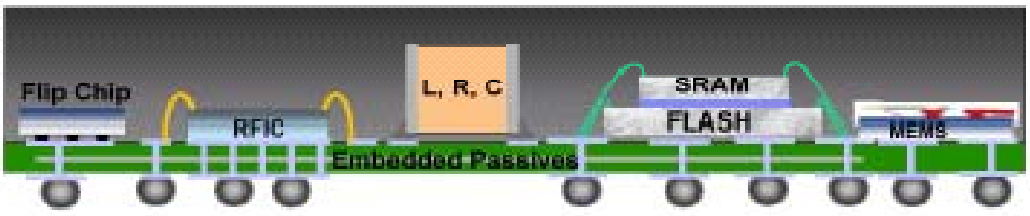
MCM vs PCB

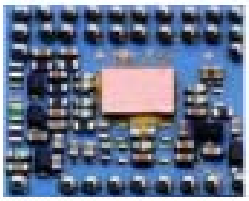
- RISC processor on PCB
- Same Electrical Circuit on MCM



System on Package: A system on u-board

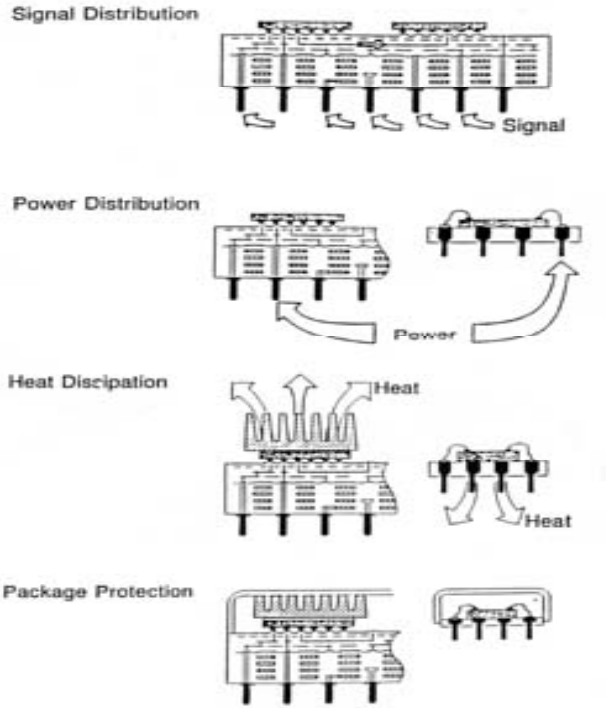






Major Function of Packaging

- Signal Distribution
- Power Distribution
- Heat Dissipation(Cooling)
- Protection
  - mechanical,
  - chemical,
  - electromagnetic



Characteristics of a package

- Packaging Efficiency

$$F_p = \frac{A_{SC}}{A_p}$$

  - Is ratio of functional area to nonfunctional area Fp is packaging efficiency; ASC - silicon chip area; Ap is package area
  - DIPs on PWB have a silicon efficiency of 1 to 3%
  - SMDs can increase it to 6 to 14%.
  - MCM-D package can take it up to 60%
- Lead Count
  - In-line packages : 8 – 40 leads
  - Small outline packages : 24 – 64 leads
  - Quad packages : 64 – 200 leads
  - Array packages : > 200 leads to 3000

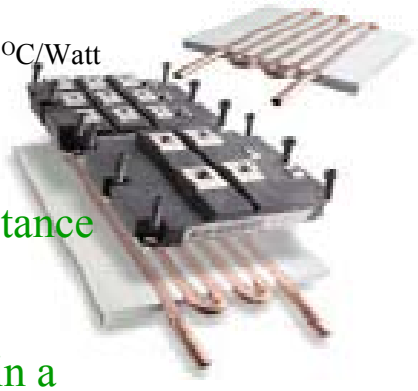
Characteristics of a package

- Thermal Performance
  - Characterized by the thermal resistance, $^{o}C/Watt$

$$T_{junction} = T_{ambient} + q_{JA}.P$$

$$q_{JA} = q_{JC} + q_{CA}$$

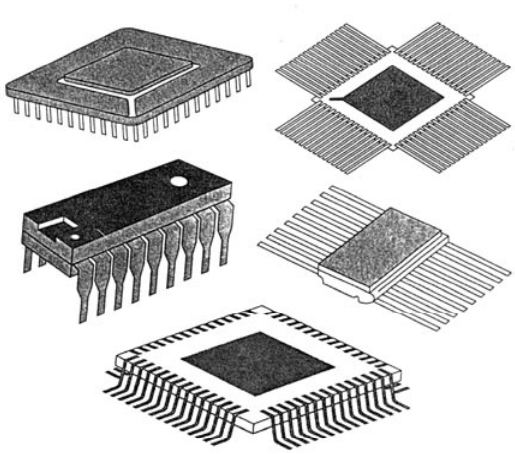
  - Ceramic bodies give lower thermal resistance
  - High-power ICs use heat sinks
  - 7 x 7 mm chip dissipating 30 W results in a heat flux of more than 6×10^5 W/m^2
- Electrical Performance
  - Delay
  - Cross Talk
  - Power Distribution



Case to Ambient Thermal Resistance:
16-pin DIP in still air 80^{o}C/W
Junction to Case Thermal Resistance:
16-pin DIP in still air 34^{o}C/W

Characteristics of a package

- Size and Weight
  - Smaller size leads to higher silicon efficiency: BGA and CS packages
  - Weight reduction is only through the choice of materials.
  - Plastic bodies have less weight than Ceramic bodies
  - 40-pin plastic DIP weighs about 6 gms



–40-pin ceramic DIP weighs about 12 gms

–196-lead plastic quad flat pack weighs about 9 gms.

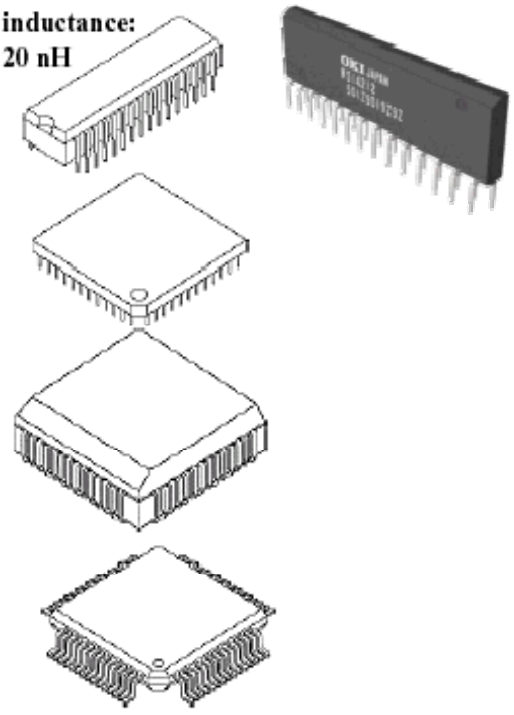
Characteristics of a package

- Reliability
  - Reliability is influenced by
    - Choice of materials
    - Manufacturing processes
    - Operating conditions and environment
  - Reliability is enhanced by
    - Hermetic packages
    - Derating the devices
    - Protecting interconnection with organic coatings
    - Controlling the environment ambient to the device

Package Evolution

- DIL (Dual In Line)
  - Low pin count
  - Large
- PGA (Pin Grid Array)
  - High pin count (up to 400)
  - Previously used for most CPU's
- PLCC (Plastic leaded chip carrier)
  - Limited pin count (max 84)
  - Large
  - Cheap
  - SMD
- QFP (Quarter Flat pack)
  - High pin count (up to 300)
  - small
  - Cheap
  - SMD

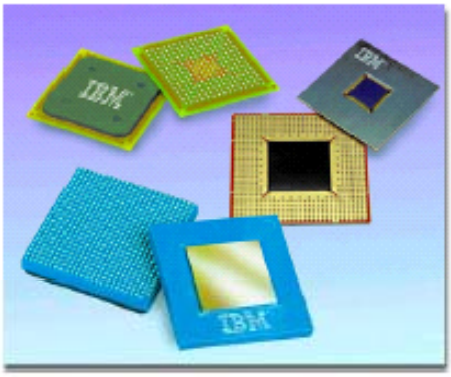
Package inductance:
1 - 20 nH

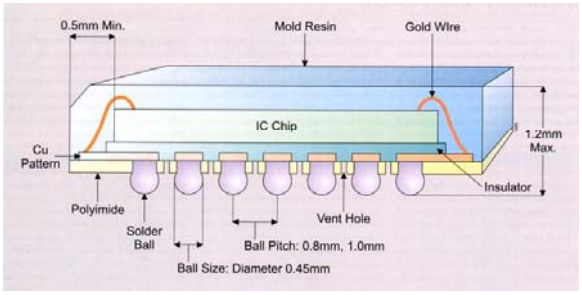


Package Evolution

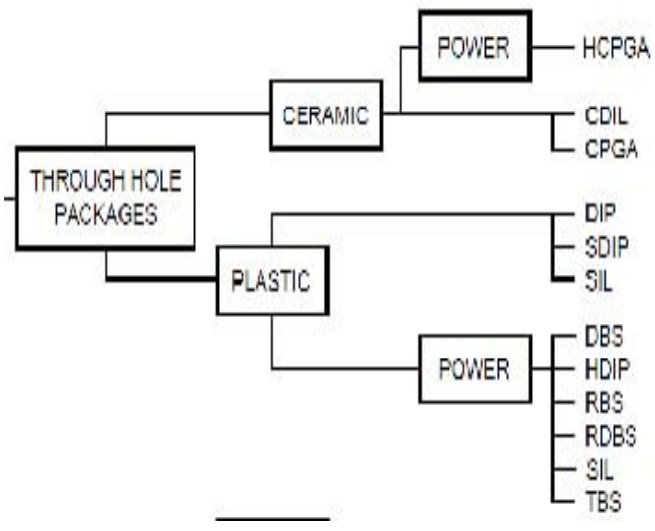
- BGA (Ball Grid Array)
  - » Small solder balls to connect to board
  - » small
  - » High pin count
  - » Cheap
  - » Low inductance
- CSP (Chip scale Packaging)
  - » Similar to BGA
  - » Very small packages

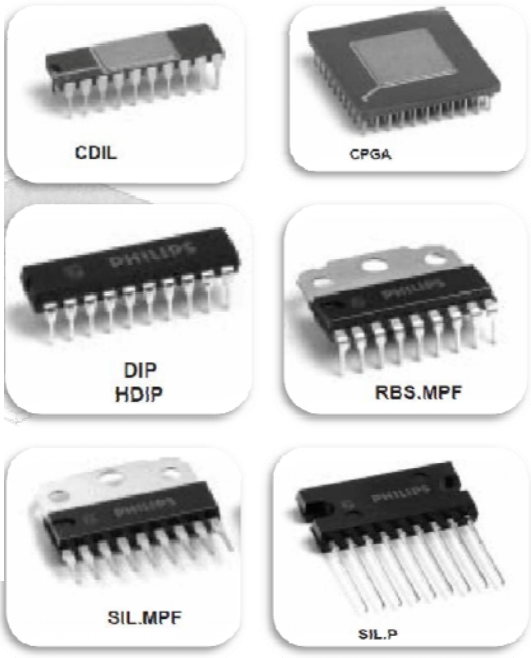
Package inductance:
1 - 5 nH



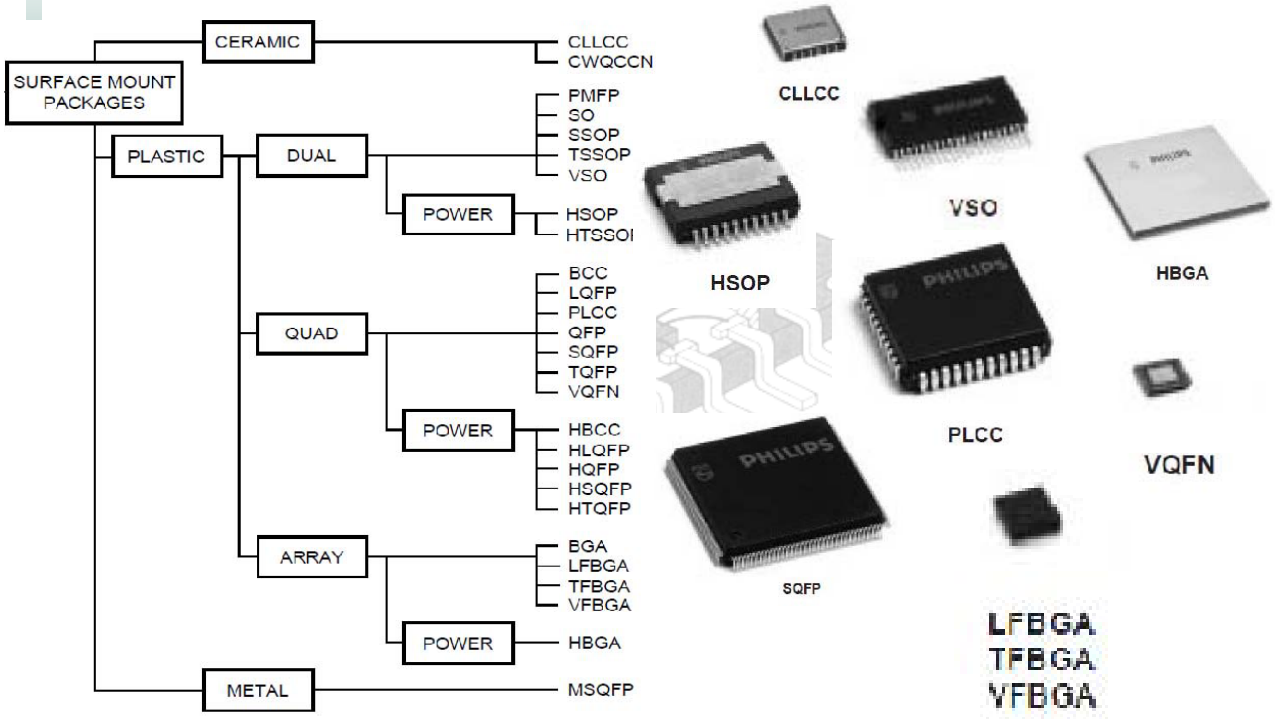


Types of Through Hole packages



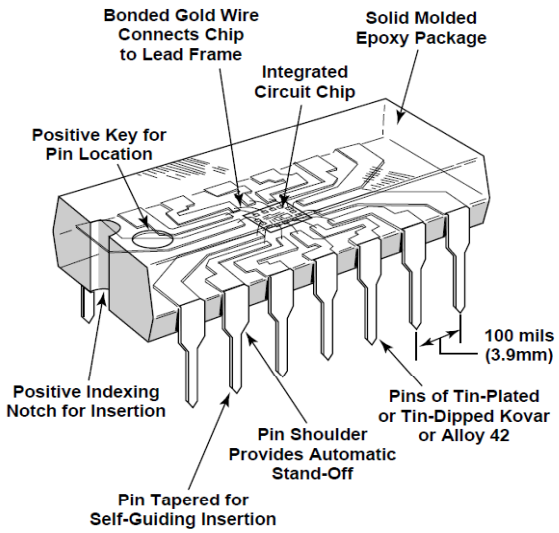


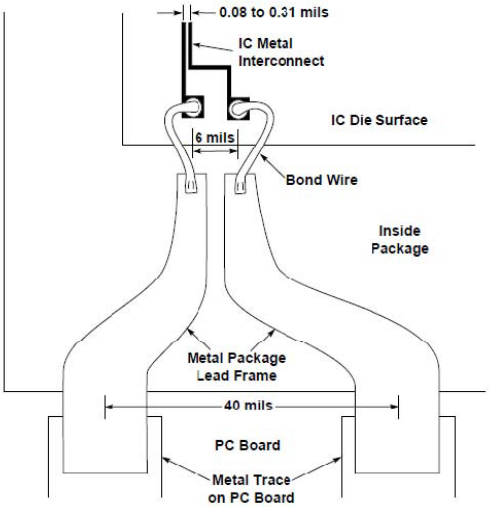
Types of Surface Mount Packages



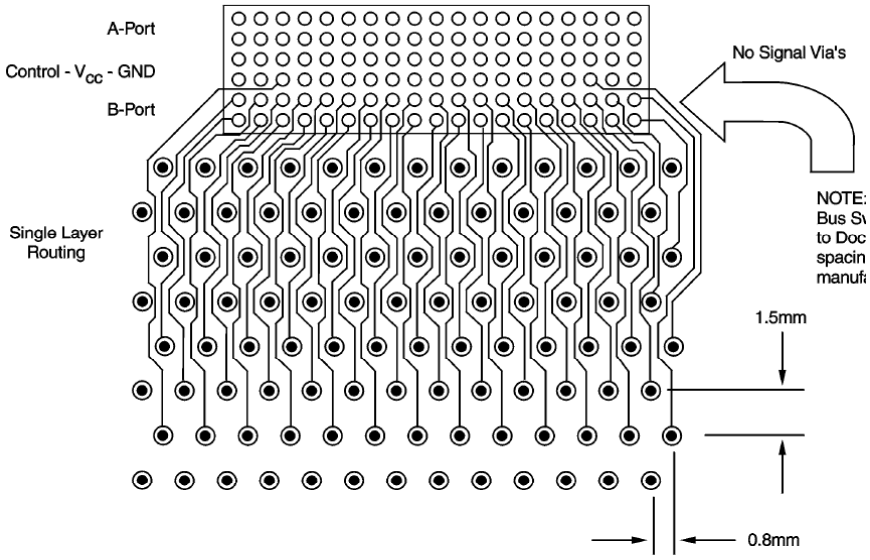
Packaging Efficiency

- Ratio between die area and package area
- Ranges from 5% (DIP) to 90% (BGA,CSP)
- BGA Bond Pads are ≈50µm apart





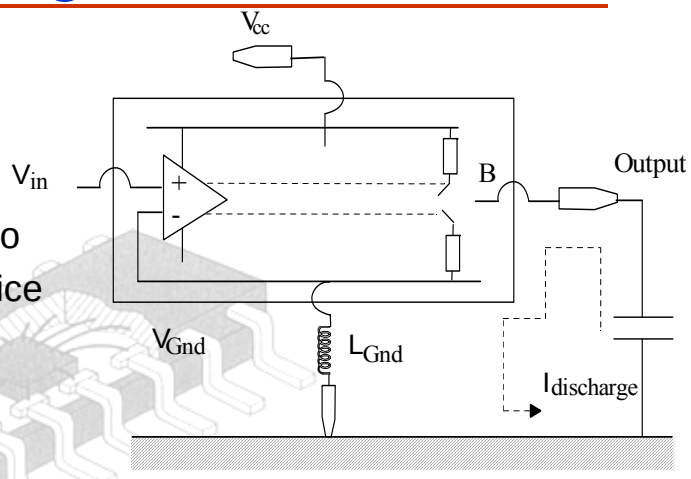
Routing Complexity α Package Type



Packaging Effects

- GND Bounce (Inductance)
  - Ground bounce problem due to lead inductance of a logic device
  - Ground bounce voltage

$$V_{GND} = L_{GND}. dI_{discharge}/dt$$



14 pin plastic DIP	8	nH
68-pin plastic DIP	35	nH
68-pin SM plastic PLCC	7	nH
Wire bonded to hybrid substrate	1	nH
Solder bump to hybrid substrate	0.1	nH

Packaging Effects

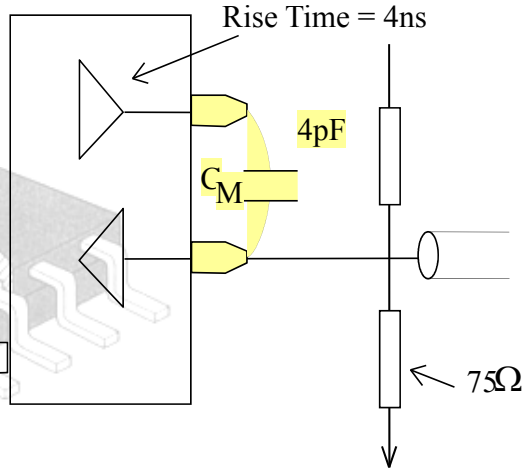
Some typical IC packages and their lead inductances			
14-pin DIP	3.2 - 10.2 nH	14-pin SOIC	2.6 - 3.6 nH
20-pin DIP	3.4 - 13.7 nH	20-pin SOIC	4.9 - 8.5 nH
40-pin DIP	4.4 - 21.7 nH		
40-pin TAB	1.2 - 2.5 nH	208-pin QFP	5.31 - 8.74 nH
44-pin QFP	6.07 - 7.06 nH	100-pin QFP	6.69 - 7.96 nH
20-pin PLCC	3.5 - 6.3 nH	119-pin PBGA	.15 - 5.7 nH
28-pin PLCC	3.7 - 7.8 nH	249-pin PBGA	.13 - 5.1 nH
44-pin PLCC	4.3 - 6.1 nH	624-pin CBGA	.5 - 4.75 nH
68-pin PLCC	5.3 - 8.9 nH	456-pin PBGA	.2 - 5.8 nH

Packaging Effects

- Cross Talk (Capacitance)

Crosstalk = R_2C_M/T_r

- C_M = 4 pF, R_2 = 37.5 ohms and T_r = 5 ns
- Capacitive crosstalk = 0.03 (3%)



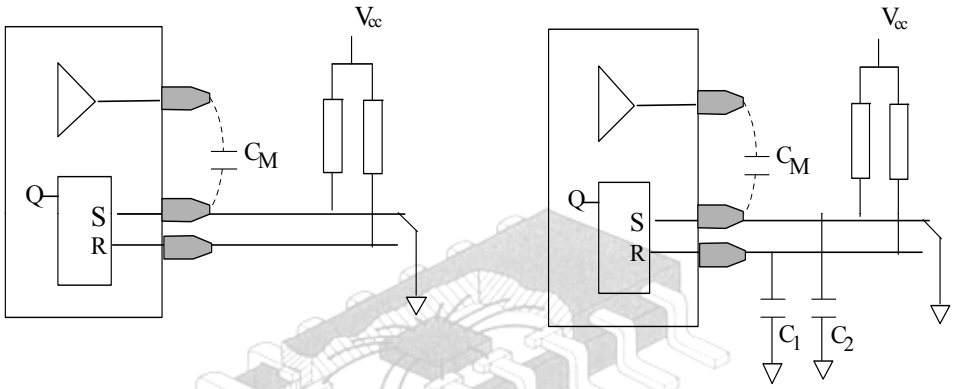
14-pin plastic DIP 4pF

68-pin SM PLCC 7pF

Wire bonded to hybrid substrate1pF

Solder bump to hybrid substrate 0.5 pF

Packaging Effects



- High-impedance input problem:

Without C1 and C2 the impedance of R1 & R2 are high (~10k)Crosstalk factor = 8

C1 and C2 reduce the impedance of the receiving circuit at high frequencies

Crosstalk factor = $C_M/C1$.

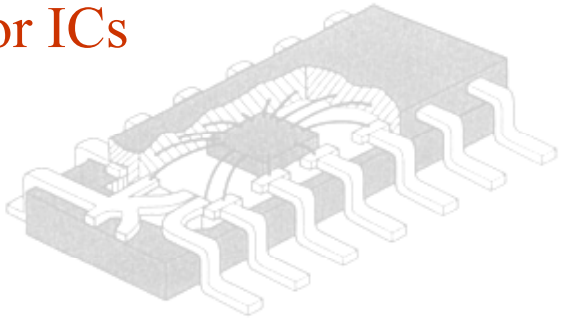
If C1 is set to 0.01 mF, crosstalk = 0.0004.

Package W.R.T Routing

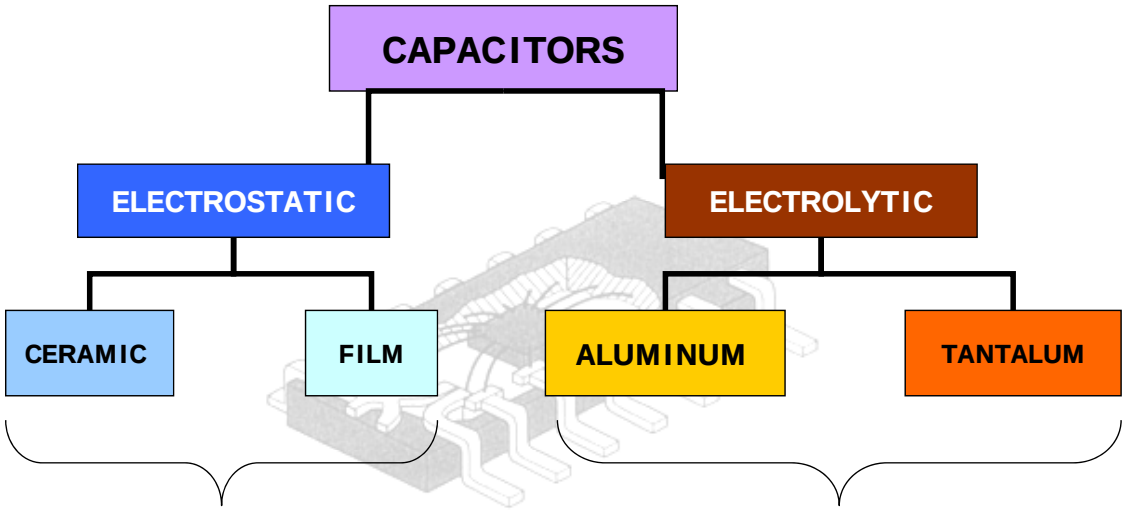
- The pitch of package determines the Routing GRID
- Routing Grid should be integral multiple or sub-multiple of the package pitch.

Packages Types

- Packages for passive components
- Package for discrete components
- Package for ICs



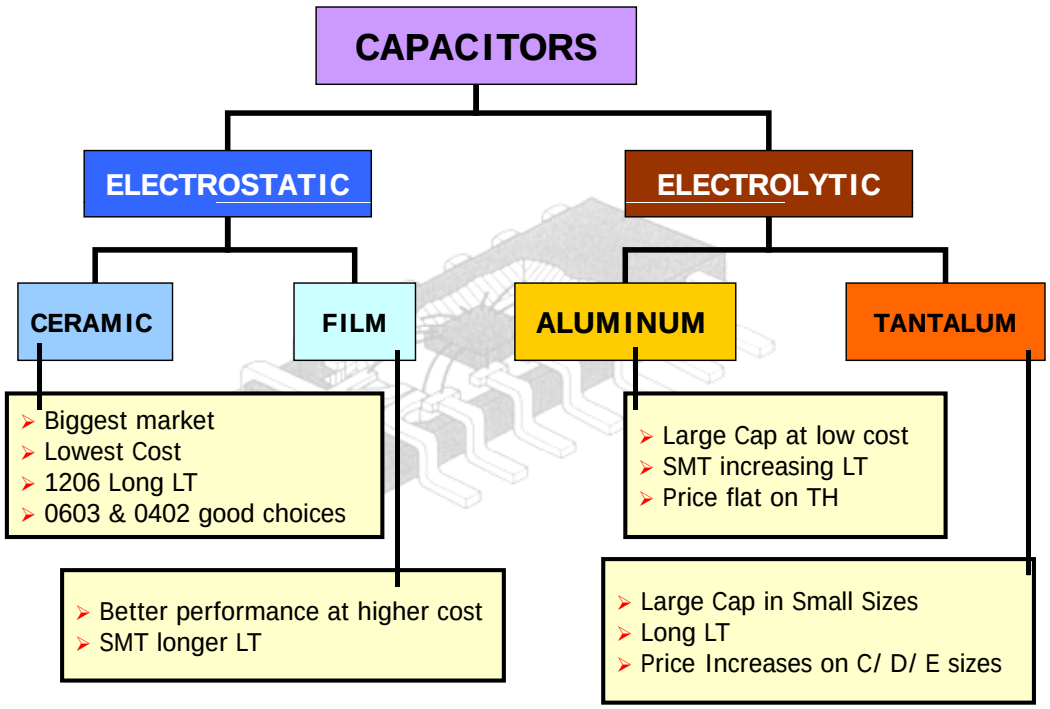
Capacitor Family Tree



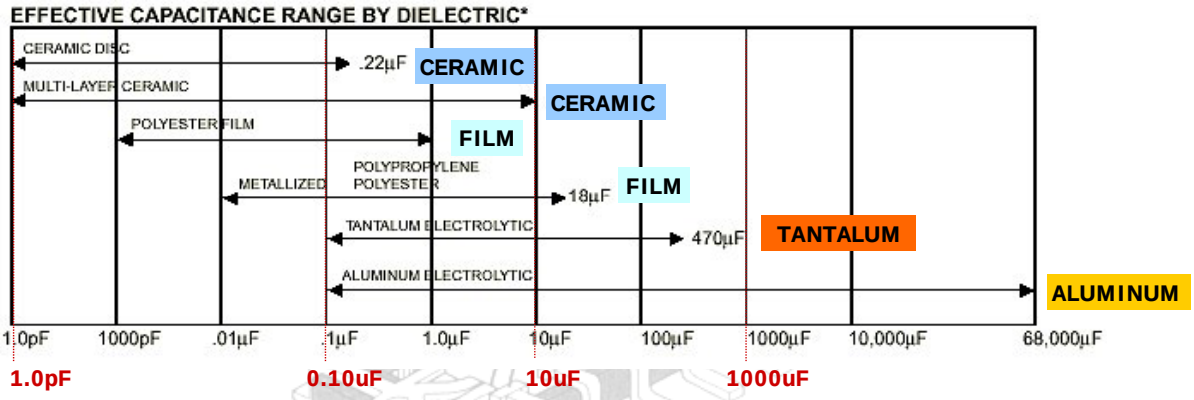
- **Non polarized**
- **AC or DC operation**
- **Lower Capacitance**

- **Polarized**
- **DC operation**
- **Higher Capacitance**

Capacitor Family Tree



Capacitor Values



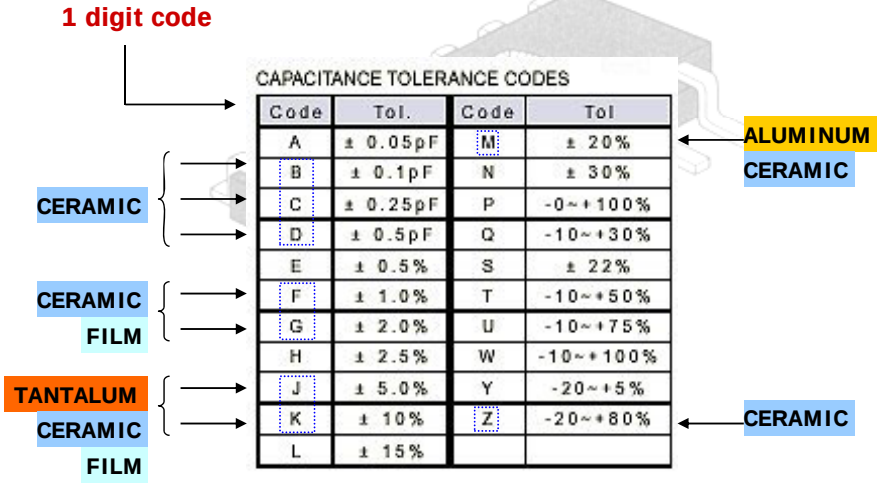
ALUMINUM } µF = *micro-Farad* = 1 x 10^{-6} F = 1 millionth of a Farad

nF = *Nano-Farad* = 1 x 10^{-9} F = 1 billionth of a Farad

TANTALUM
CERAMIC
FILM } pF = *Pico-Farad* = 1 x 10^{-12} F = 1 trillionth of a Farad

Capacitor Tolerance

The allowable window - limits that the capacitors' +25°C (room temperature) capacitance value will be within.



Code	Tol.	Code	Tol
A	± 0.05pF	M	± 20%
B	± 0.1pF	N	± 30%
C	± 0.25pF	P	-0~+100%
D	± 0.5pF	Q	-10~+30%
E	± 0.5%	S	± 22%
F	± 1.0%	T	-10~+50%
G	± 2.0%	U	-10~+75%
H	± 2.5%	W	-10~+100%
J	± 5.0%	Y	-20~+5%
K	± 10%	Z	-20~+80%
L	± 15%		

Thermal Characteristics

Standard Temperature Coefficients (TC) of ceramic capacitors:

Low Temperature Limit	High Temperature Limit	Maximum Allowable Capacitance Change From +25°C (0 VDC)
X = -55°C	5 = +85°C	F = ±7.5%
Y = -30°C	6 = +105°C	P = ±10%
Z = +10°C	7 = +125°C	R = ±15%
	8 = +150°C *(SPECIAL)*	S = ±22%
		T = +22% / -33%
		U = +22% / -56%
		V = +22% / -82%

X7R = ±15% ΔC over -55°C ~ + 125°C

Aluminum Electrolytic styles have TC of±20% over -40°C to +105°C

Tantalum Electrolytic styles have TC of ±5% over -55°C to +85°C

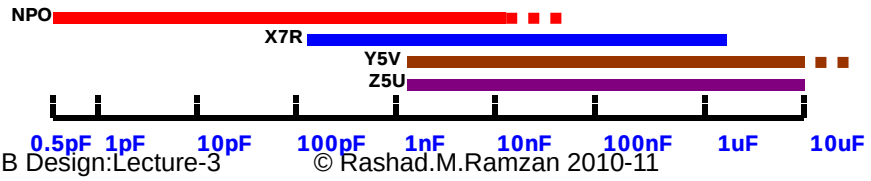
Film styles have TC of ±7% over -40°C to +105°C

Capacitor Range

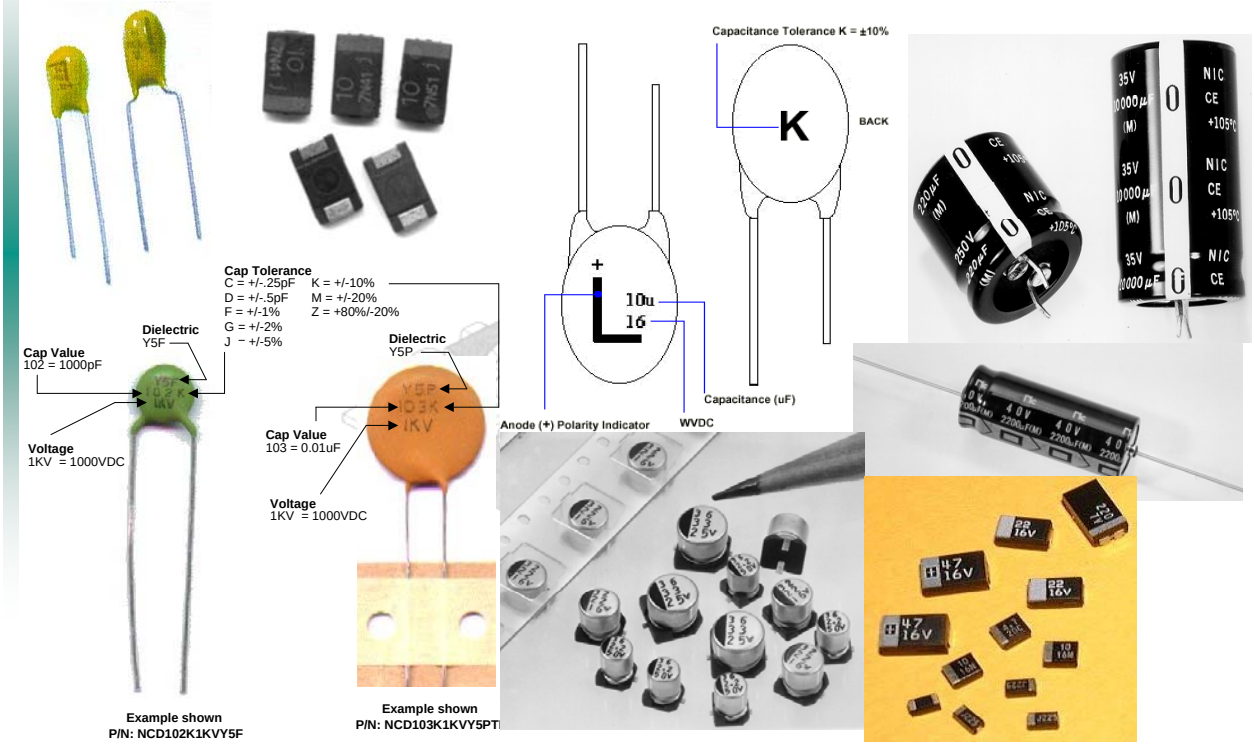
Multilayer Ceramic Chip Capacitor

Temperature Coefficients:

TC	Capacitance Range	Capacitance Value Code	Voltage Range	Standard Tolerance
NPO	0.5pF ~ 0.056uF	0R5 ~ 563	25VDC ~ 1KVDC	(J) +/-5%
X7R	100pF ~ 2.2uF	101~ 225	16VDC ~ 1000VDC	(K) +/-10%
Y5V	1000pF ~ 10uF	102 ~ 106	16VDC ~ 50VDC	(Z) -20%/+80%
Z5U	1000pF ~ 10uF	102 ~ 106	16VDC ~ 50VDC	(M) +/-20%

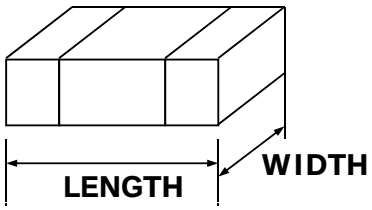


Capacitor packages



Capacitor Dimensions SMD

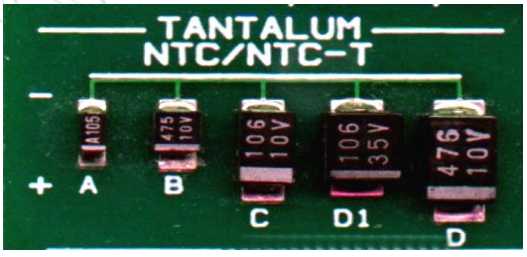
English	Metric	Length	Width
0402	1005	1.0mm (0.04”)	0.5mm (0.02”)
0603	1608	1.6mm (0.06”)	0.8mm (0.03”)
0805	2012	2.0mm (0.08”)	1.2mm (0.05”)
1206	3216	3.2mm (0.12”)	1.6mm (0.06”)
1210	3225	3.2mm (0.12”)	2.5mm (0.10”)
1812	4532	4.5mm (0.18”)	3.2mm (0.12”)
2225	5764	5.7mm (0.22”)	6.4mm (0.25”)



Surface Mount Tantalum Electrolytic Capacitors

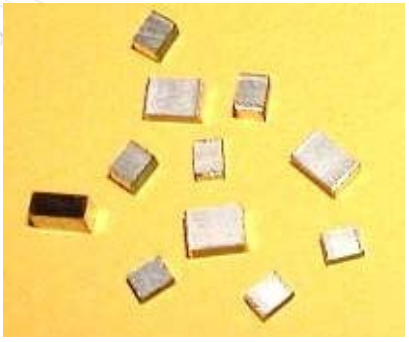
Case Code	Metric	English	Length	Width
P	2012	0805	2.0mm (0.08”)	1.2mm (0.05”)
A, A2	3216	1206	3.2mm (0.12”)	1.6mm (0.06”)
B, B2	3528	1411	3.5mm (0.14”)	2.8mm (0.11”)
C	6032	2412	6.0mm (0.24”)	3.2mm(0.12”)
D1*	5846	2318	5.8mm (0.23”)	4.6mm(0.18”)
D, E	7343	2917	7.3mm (0.29”)	4.3mm (0.17”)

* - *D1 is Japanese size*



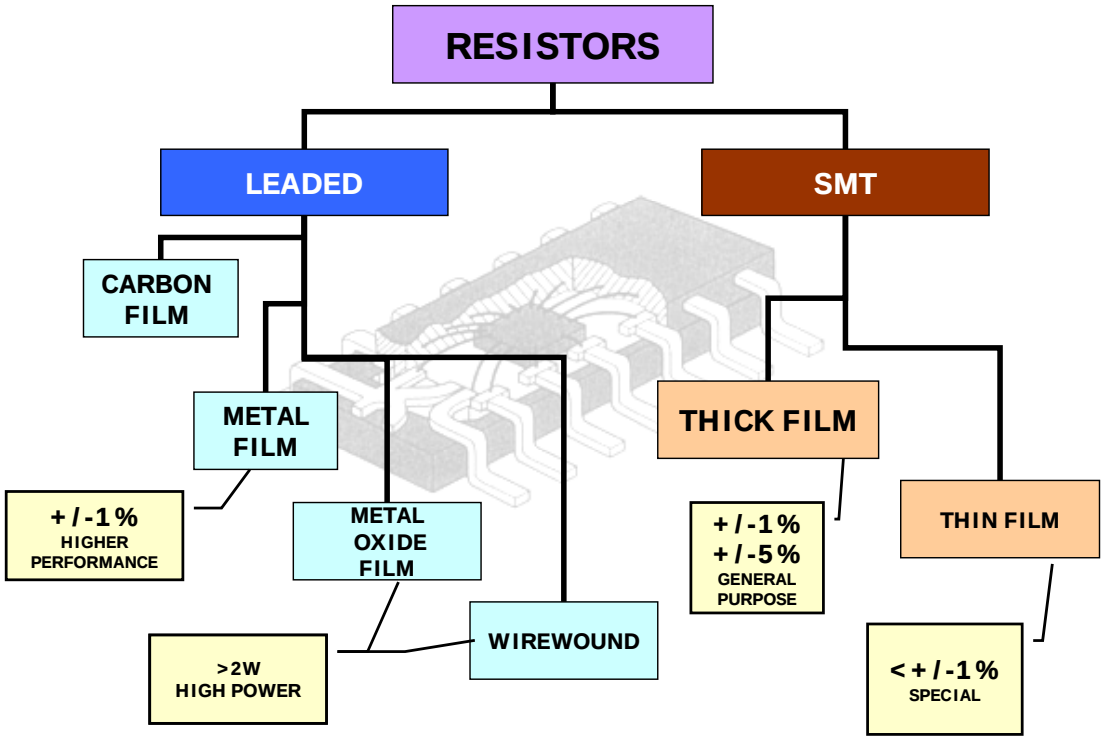
Surface Mount Film Chip Capacitors

English	Metric	Length	Width
0805	2012	2.0mm (0.08”)	1.2mm (0.05”)
1206	3216	3.2mm (0.12”)	1.6mm (0.06”)
1210	3225	3.2mm (0.12”)	2.5mm (0.10”)
1913	4833	4.8mm (0.19”)	3.3mm (0.13”)
2416	6041	6.0mm (0.24”)	4.1mm (0.16”)

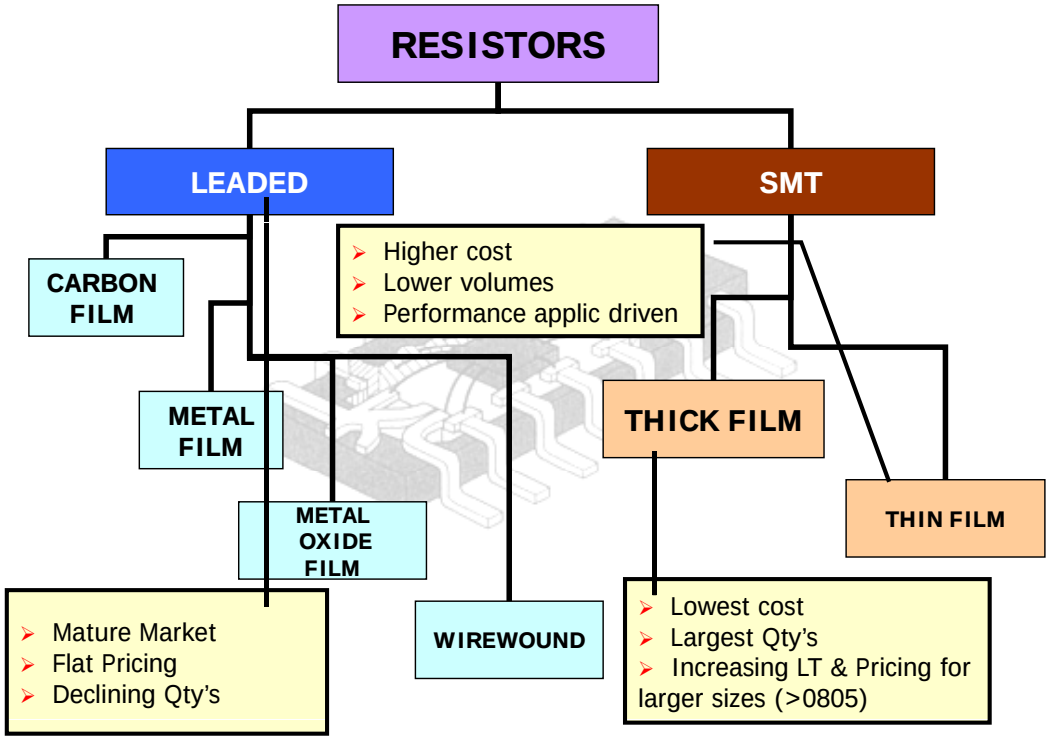


No Component Marking

Resistor Family Tree

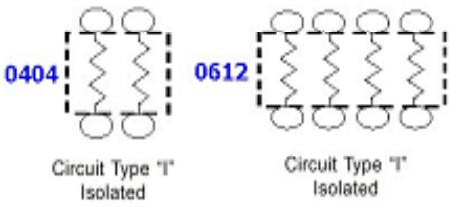


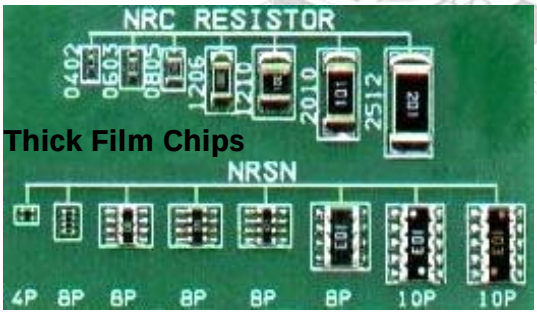
Resistor Family Tree

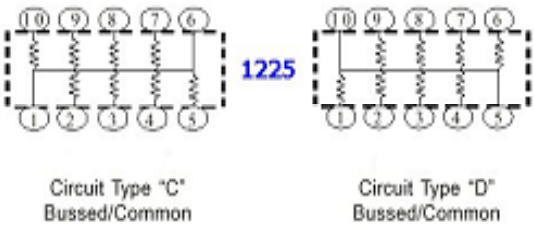


SMD Resistor Sizes

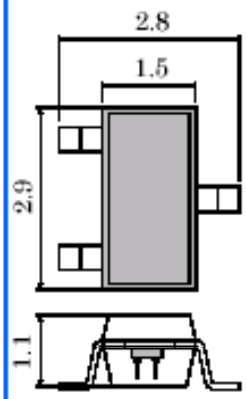
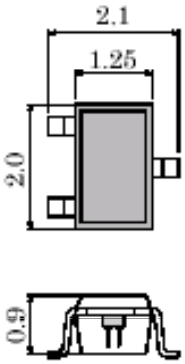
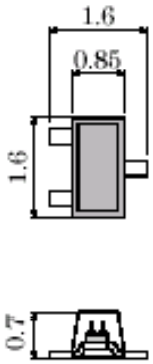
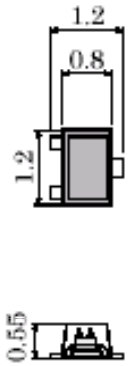
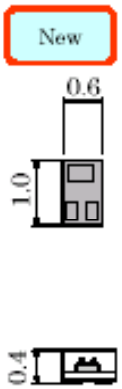
English	Metric	Length	Width
0201	0502	0.5mm (0.02")	0.25mm (0.01")
0402	1005	1.0mm (0.04")	0.5mm (0.02")
0603	1608	1.6mm (0.06")	0.8mm (0.03")
0805	2012	2.0mm (0.08")	1.2mm (0.05")
1206	3216	3.2mm (0.12")	1.6mm (0.06")
1210	3225	3.2mm (0.12")	2.5mm (0.10")
1812	4532	4.5mm (0.18")	3.2mm (0.12")
2225	5764	5.7mm (0.22")	6.4mm (0.25")



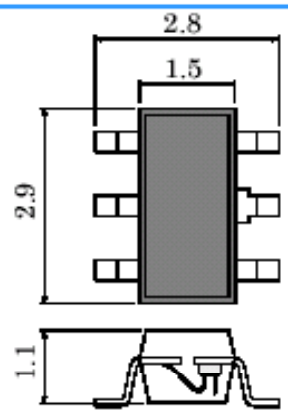
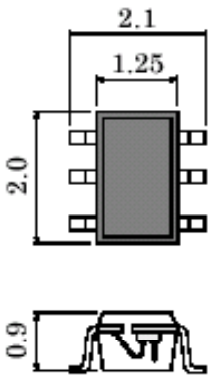
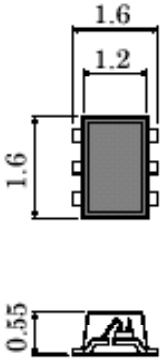
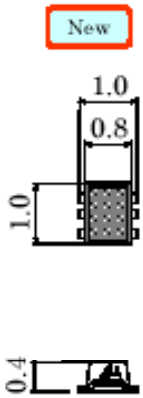




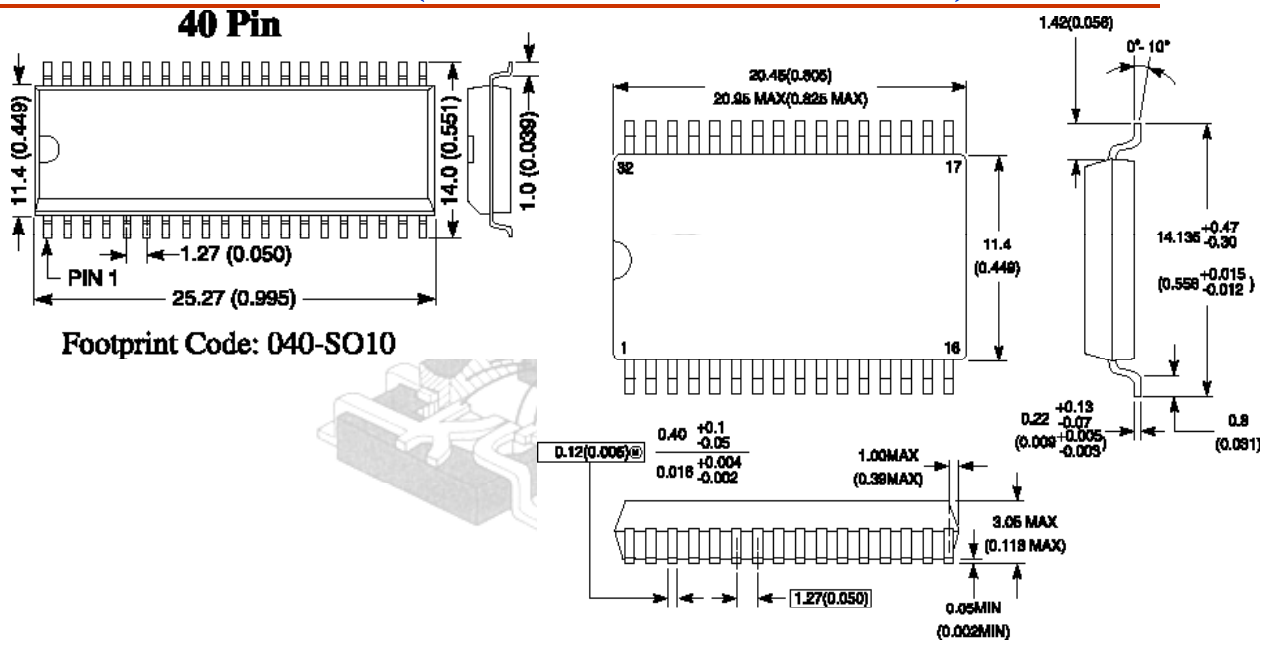
Discrete Packages

	Mini EIAJ : SC-59	S Mini EIAJ : SC-70	SS Mini EIAJ : SC-75	SSS Mini EIAJ : SC-59	1006 Lead-less
Package Dimension					
Mounting area	8.12 mm^2	4.20 mm^2	2.56 mm^2	1.44 mm^2	0.6 mm^2
Compare to SC-59	100 %	51.72 %	31.53 %	17.56 %	7.39 %
Reduction		51.72%	60.95%	56.25%	41.67%

Discrete Packages

	Mini (XN) EIAJ : SC-74	S Mini (XP) EIAJ : SC-88	SS Mini (UP)	SSS Mini (NP)
Package Dimension				
Mounting area	8.12 mm^2	4.20 mm^2	2.56 mm^2	1.00 mm^2
Compare to SC-74	100 %	51.72 %	31.53 %	12.32 %
Reduction		51.72 %	60.95 %	39.06 %

SOIC (Shrink Outline IC)



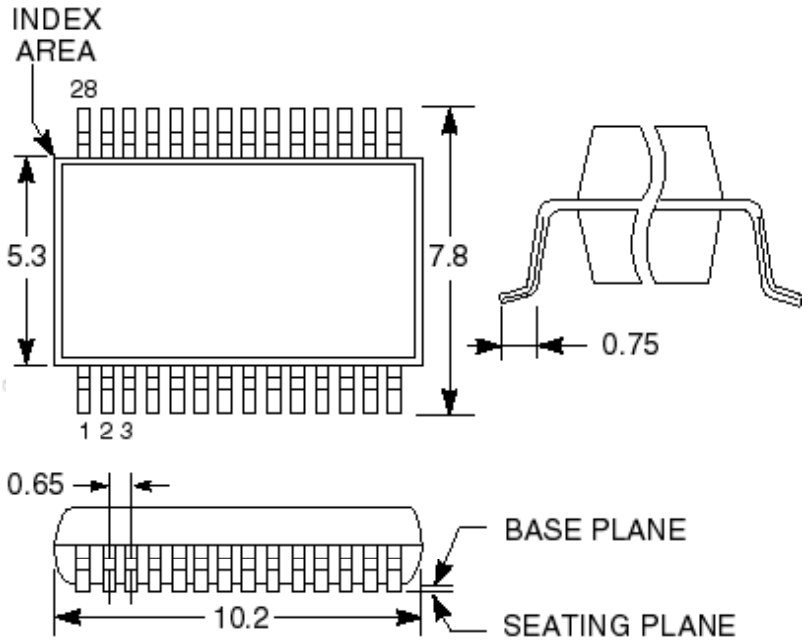
•Lead Pitch: 0.5mm, 0.65mm ,0.8mm,…

IC Package Pitch & Routing Grid

- Grid: An invisible imaginary mesh on which we can place the traces on the PCB board. Size of grid depends upon component pitch, no of traces, no of I.Os and routing space available.
- Routing the traces is preferred to be on grid.
  - Easy to rout by hand and modify.
  - Auto router performs faster on bigger grids but do not route 100% traces.
  - Easy to reroute and rip off.
- If possible choose the package with same pitch size or some even multiple factor.

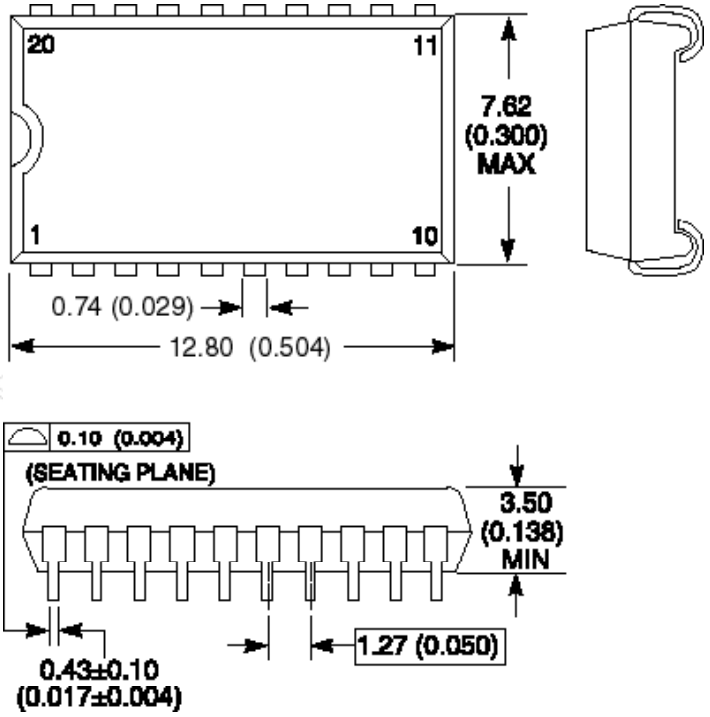
SSOP (Small Shrink Outline Pack)

- Lead Pitch:
  - 0.5mm
  - 0.65mm
  - 0.8mm…



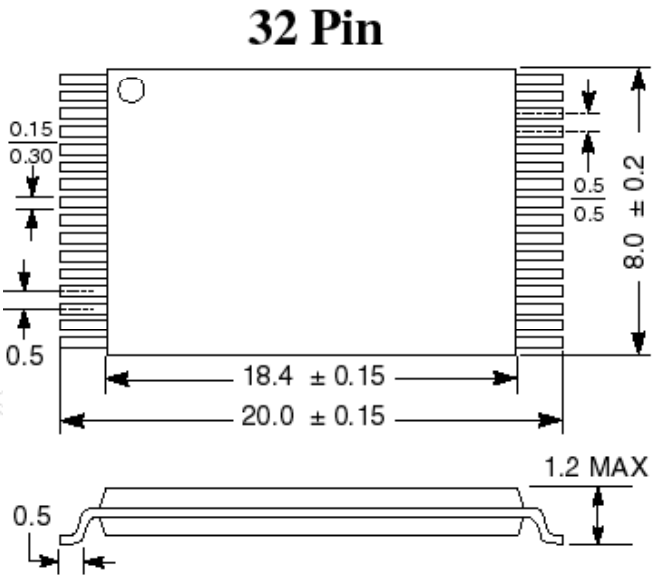
SOJ (Shrink Outline J Leaded)

- Lead Pitch:
  - 0.5mm
  - 0.65mm
  - 0.8mm…



TSOP (Thin Shrink Outline Package)

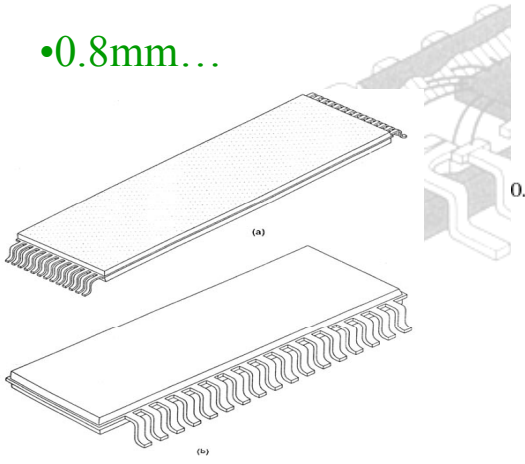
- Lead Pitch:
  - 0.5mm
  - 0.65mm
  - 0.8mm…

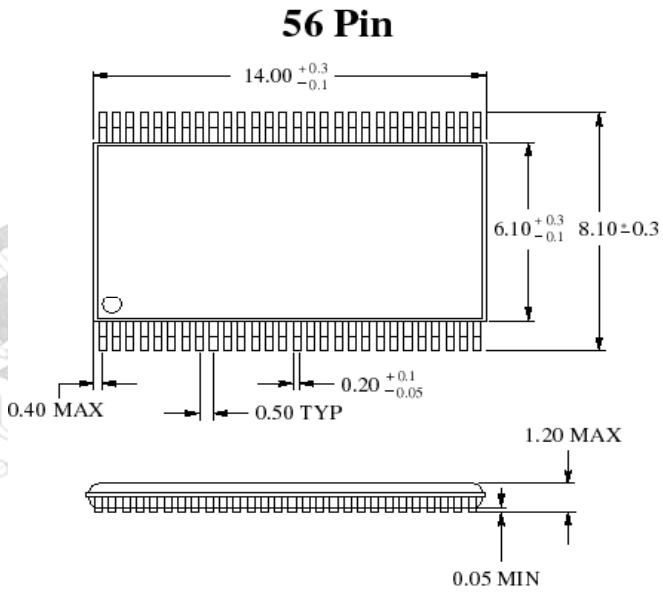


Footprint Code: 032-TS01

TSSOP (Thin Small SOP)

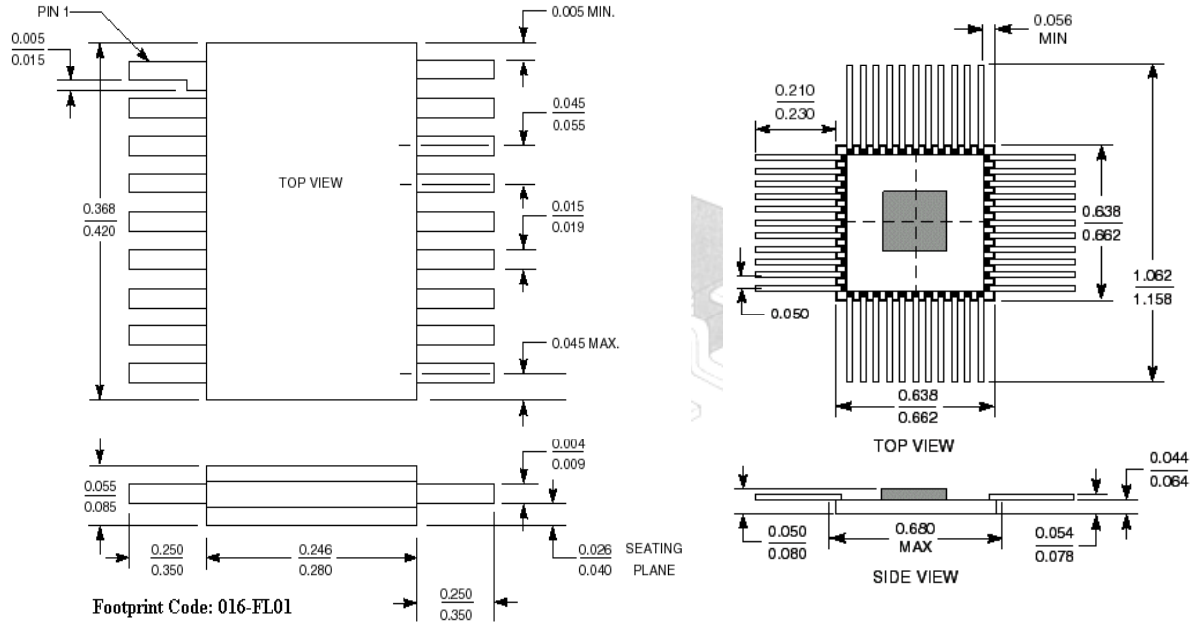
- Lead Pitch:
  - 0.5mm
  - 0.65mm
  - 0.8mm…





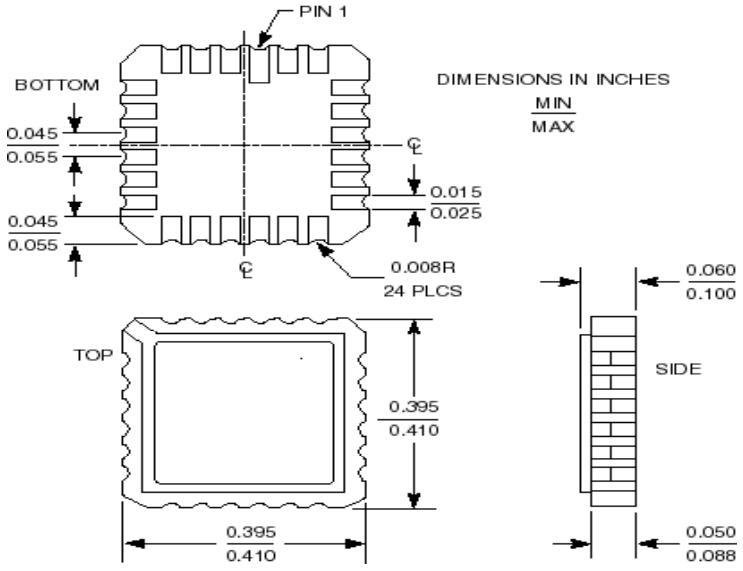
Footprint Code: 056-ST01

Flat-pack Footprints



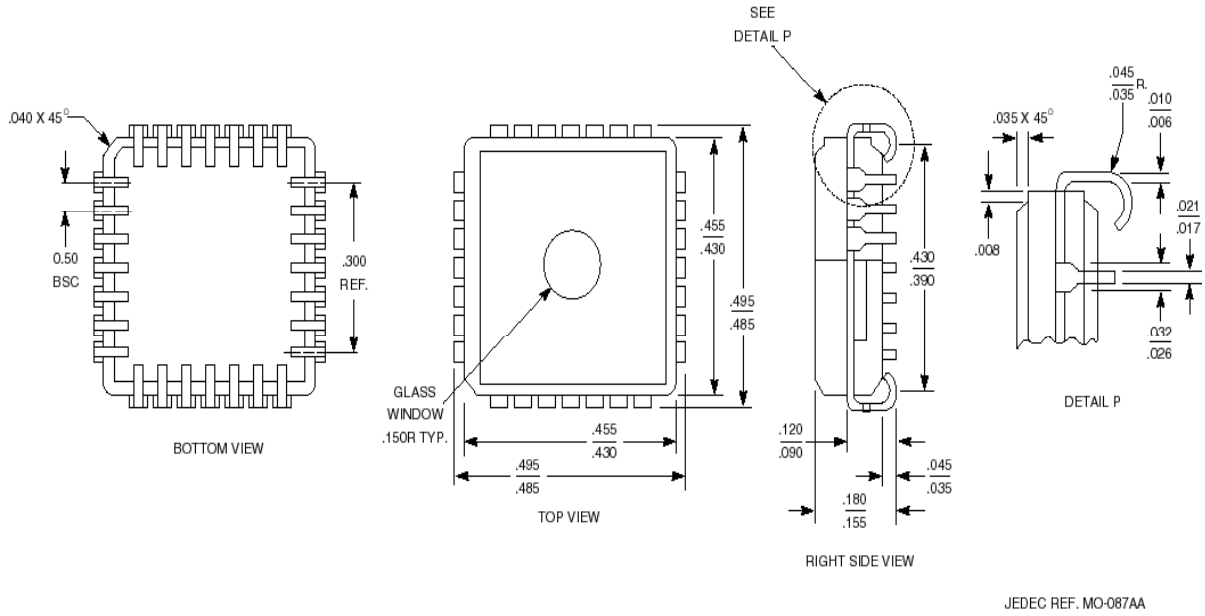
•Lead Pitch: 0.5mm, 0.65mm ,0.8mm,…

LCC (Lead Less Chip Carrier)



•Lead Pitch: 0.5mm, 0.65mm ,0.8mm,…

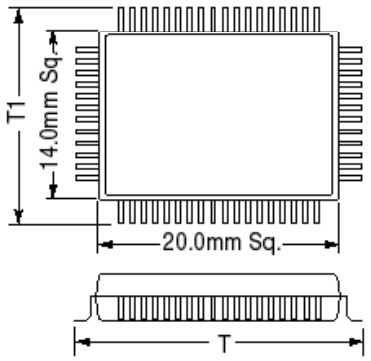
JLCC (J Leaded Chip Carrier)



•Lead Pitch: 0.5mm, 0.65mm ,0.8mm,…

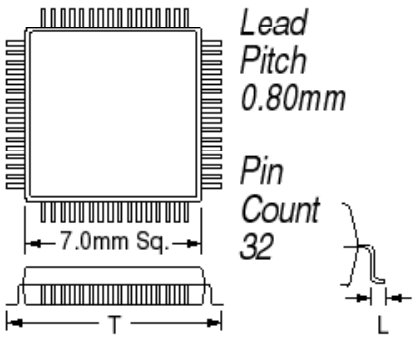
PQFP-QFP (Quad Flat Pack)

80 Pin



ET Footprint Code	Footprint Type	T / T1 = Tip to Tip Dimension (mm)	L = Foot Length (mm)
80-QF08	A	23.9 / 17.9	0.80
80-QF08	B	23.2 / 17.2	0.80
80-QF08C	C	22.6 / 16.6	0.50
80-QF08D	D	22.0 / 16.0	0.50

32 Pin

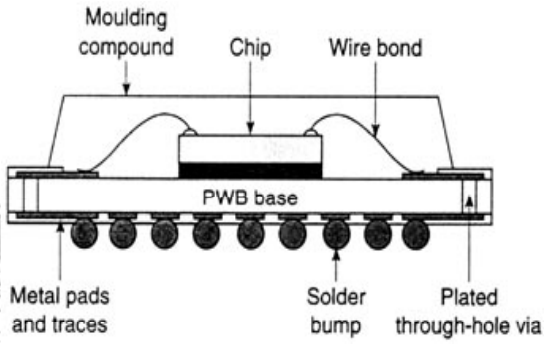


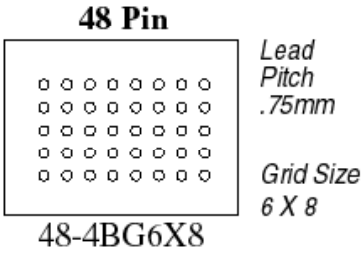
ET Footprint Code	Footprint Type	T = Tip to Tip Dimension (mm)	L = Foot Length (mm)
32-QF59	A	10.9	0.80
32-QF59	B	10.2	0.80
32-QF59C	C	9.6	0.50
32-QF59D	D	9.0	0.50

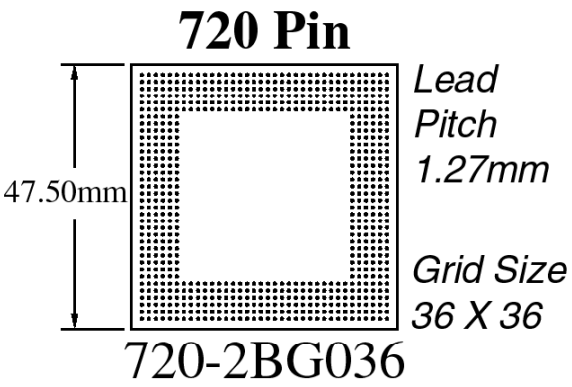
•Lead Pitch: 0.5mm, 0.65mm ,0.8mm,…

BGA (Ball Grid Array)

- Lead Pitch:
  - 0.75mm
  - 0.8mm
  - 1.0mm
  - 1.27mm
  - 1.5mm…..

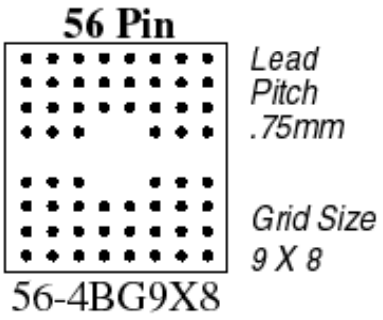


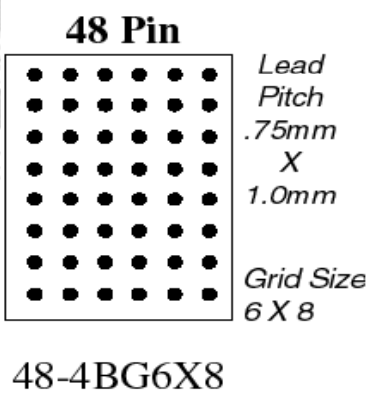




U-BGA

Pin Count	Grid Size	Lead Pitch
40	5 x 8	.75mm x 1.0mm
48	6 x 8	.75mm x 1.0mm
56	9 x 8	.75mm x 1.0mm

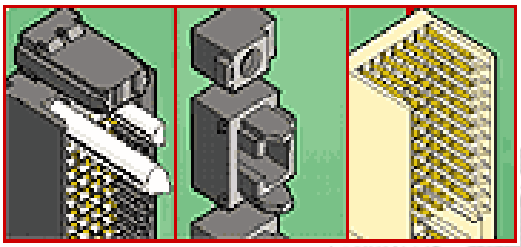




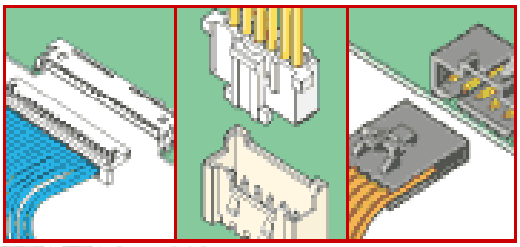
- Lead Pitch: 0.75mm, 0.8mm ,1.0mm

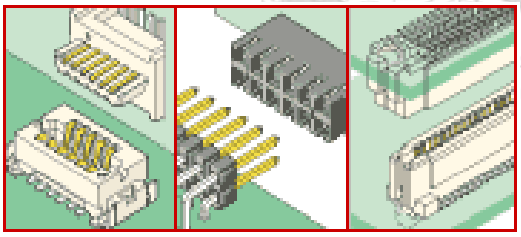
PCB Connectors: Types

- Back Plane

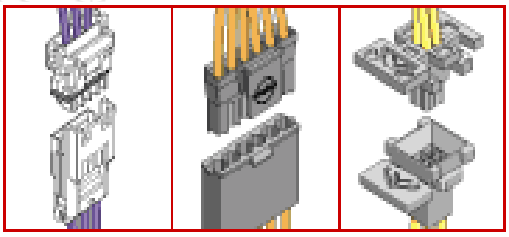


- Wire to Board





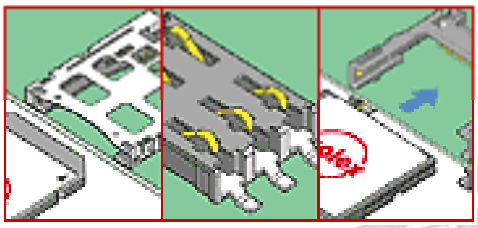
- Board to Board



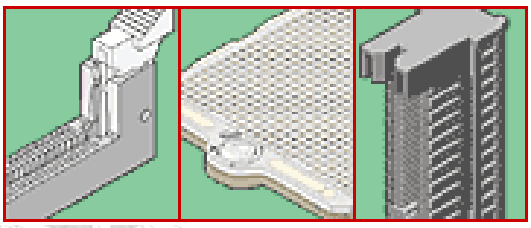
- Wire to Wire

PCB Connectors: Types

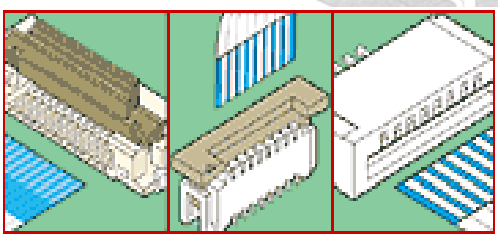
- Memory Card System



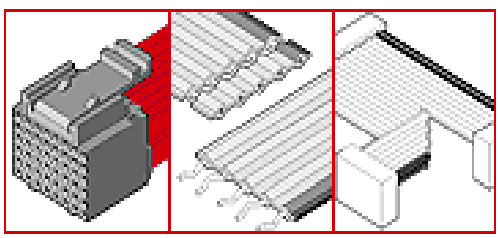
- Socket and Edge Card System Connector



- FCC FPC Connector

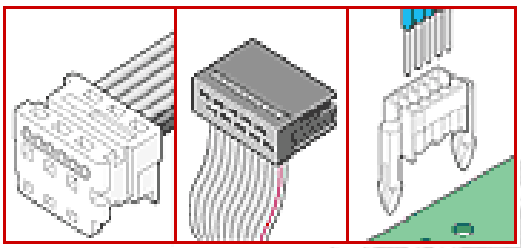


- Ribbon Cables & Jumpers

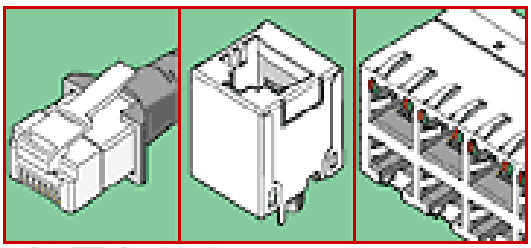


PCB Connectors: Types

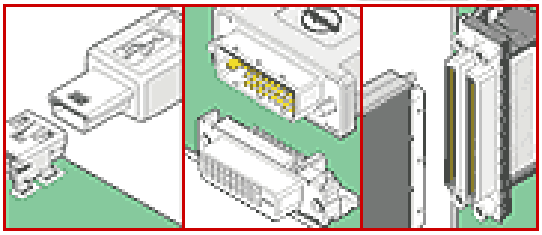
- Wire trap connector



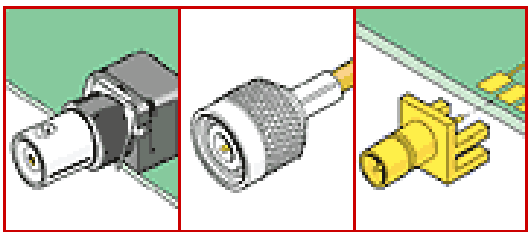
- Modular Plugs and Jacks



- Shielded Connectors

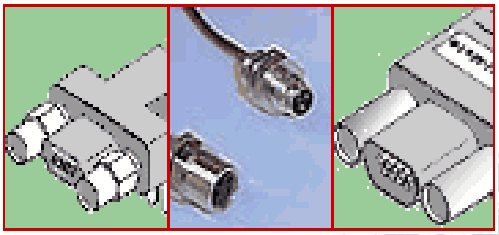


- RF- Microwave Connector

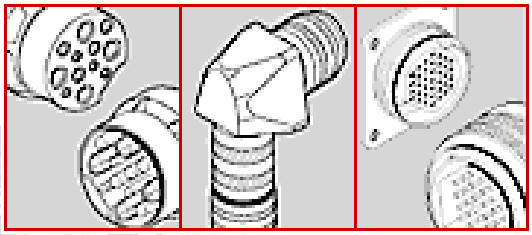


PCB Connectors: Types

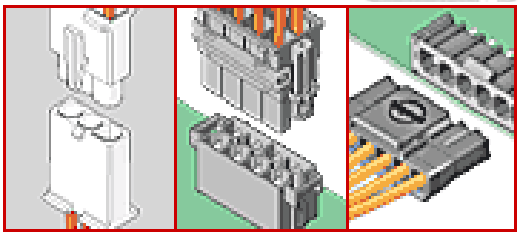
- Micro industrial



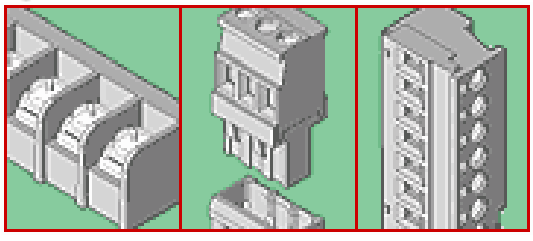
- Circular Industrial/Military



- Power Connectors

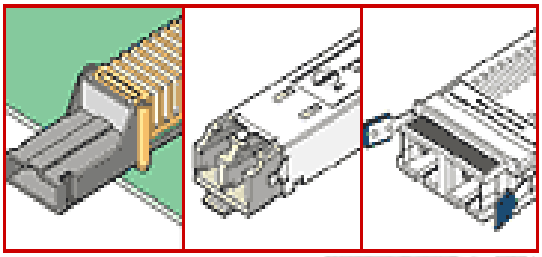


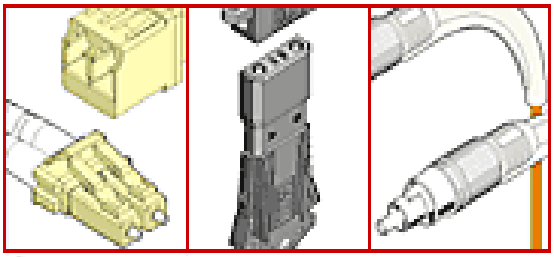
- Terminal Blocks



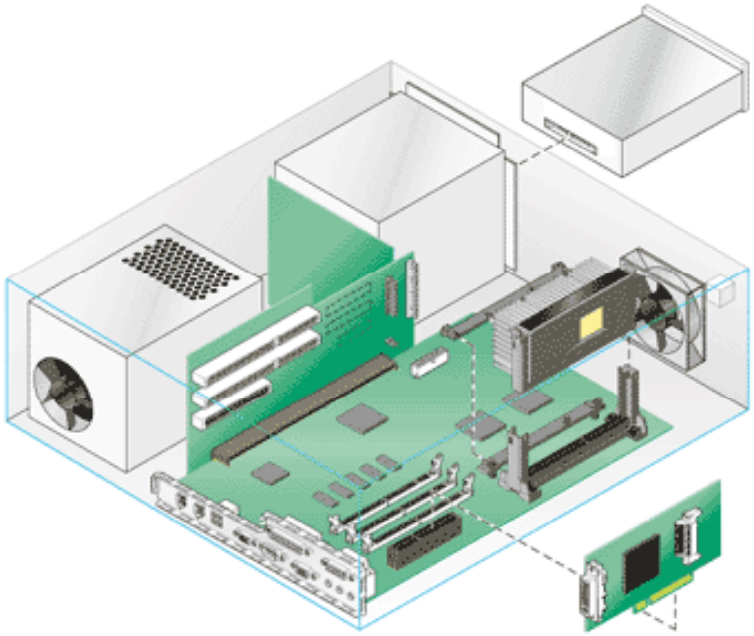
Fiber Optic Connector: Types

- Optoelectronics connectors
- Passive Connectors





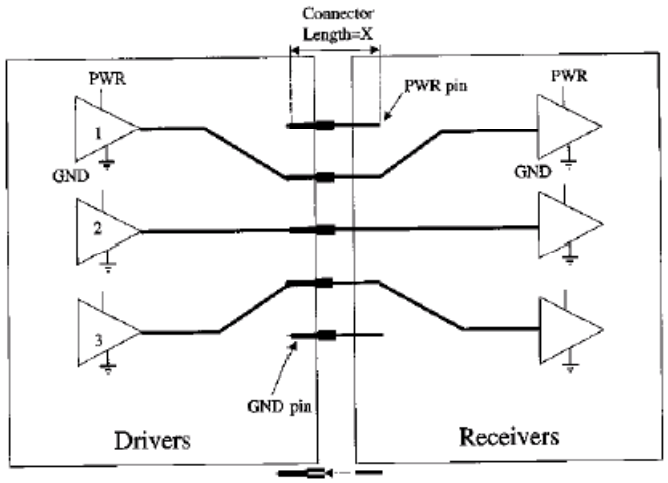
Different Type of Connectors and Cables in a Product



Connectors

$$\text{for } d \ll l\ ,\ \frac{L_s}{l} \approx \frac{\mu_o}{2\pi}\left[\ln\left(\frac{2l}{d}\right) - \frac{3}{4}\right]\ ,\ \text{else } \frac{L_s}{l} \approx \frac{\mu_o}{2\pi}\left[\ln\left(\frac{2l}{d}\right) + \frac{1}{2}\right].$$

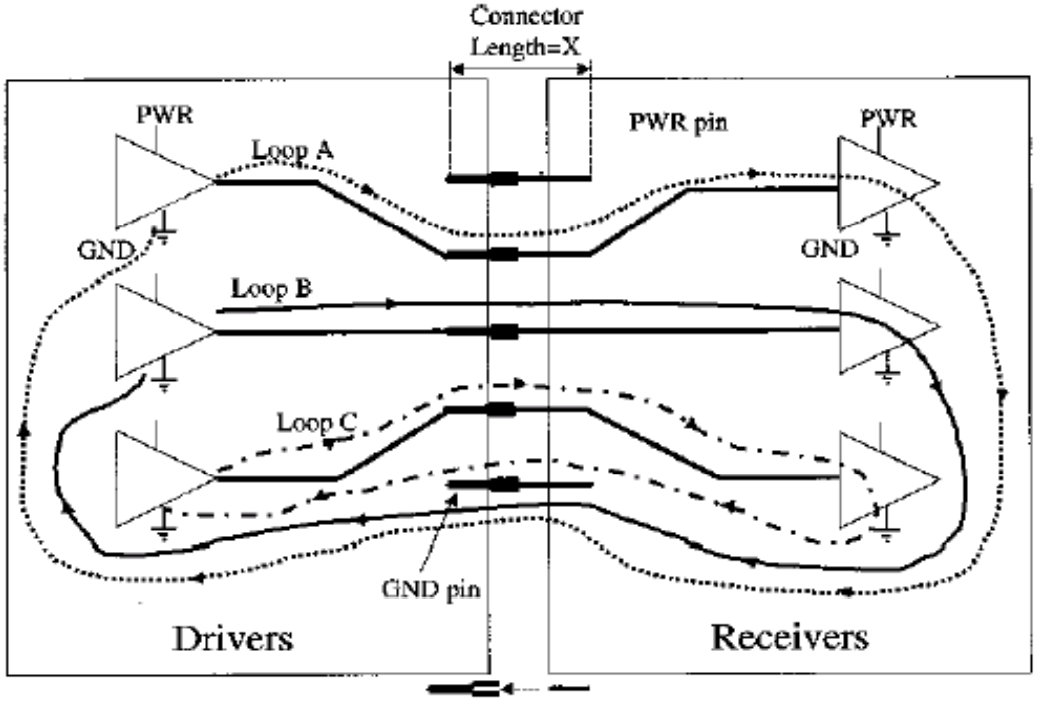
$$\text{for } s \ll l,\ \frac{L_m}{l} \approx \frac{\mu_o}{2\pi}\left[\ln\left(\frac{2l}{s}\right) - 1 + \frac{s}{2l}\right]\ ,\ \text{else } \frac{L_m}{l} \approx \frac{\mu_o}{2\pi}\left[\ln\left(\frac{l}{s} + \sqrt{1+(l/s)^2}\right) - \sqrt{1+(s/l)^2} + \frac{s}{l}\right].$$



l: length of connector pi
d: diameter of pin
s: separation of two pin

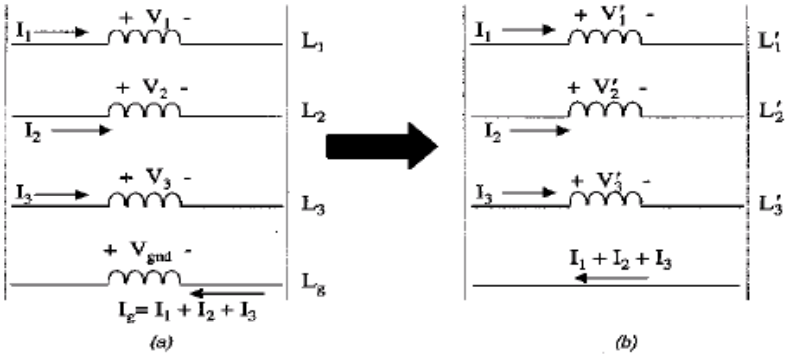
Example of a PCB connector.

Inductively Coupled Connector Pins



Current path in a connector with several drivers.

Effective Inductance of Conductor Pins



Incorporating return inductance into the signal conductor: (*a*) three inductive signal pins coupled to an inductive ground return pin; (*b*) effect of the ground return pin.

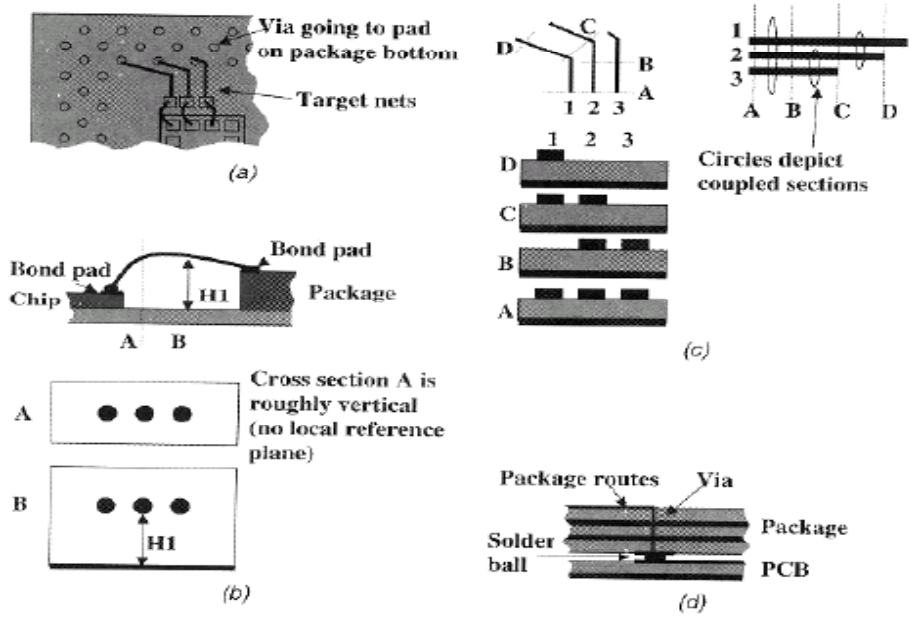
$$\begin{cases} V_2 = L_{22}\dot{I}_2 + L_{21}\dot{I}_1 + L_{23}\dot{I}_3 + L_{2g}\dot{I}_g \\ V_{gnd} = L_{gg}\dot{I}_g + L_{g1}\dot{I}_1 + L_{g2}\dot{I}_2 + L_{g3}\dot{I}_3 \\ \dot{I}_g = -(\dot{I}_1 + \dot{I}_2 + \dot{I}_3) \\ V_2' = V_2 - V_{gnd} \end{cases}$$

$$V_2' = \dot{I}_1(L_{21} - L_{2g} - L_{g1} + L_{gg}) + \dot{I}_2(L_{22} - L_{2g} - L_{g2} + L_{gg}) + \dot{I}_3(L_{23} - L_{2g} - L_{g3} + L_{gg}) = L_{22}'\dot{I}_2 + L_{21}'\dot{I}_1 + L_{23}'\dot{I}_3$$

$$L_{ij}' = L_{ij} - L_{ig} - L_{gj} + L_{gg}$$

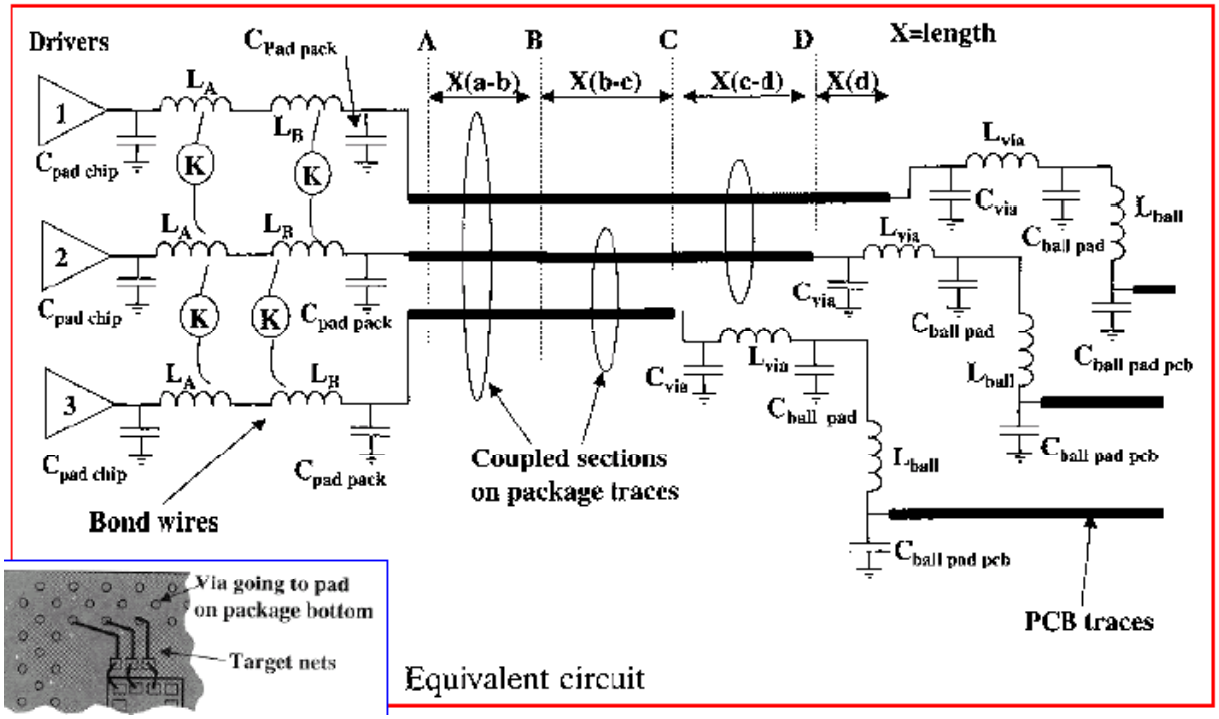
Effective inductance of each pin

Package Parasitic Modeling



Components of a package: (*a*) modeling a BGA package; (*b*) attachment of die to package; (*c*) on-package routing; (*d*) connection to PCB

Package Parasitic Modeling: EQ Circuit



Example: Connector Pin Pattern for 8-pin Pattern

G	S	S	S	S	S	S	S	S	P

(a)

G	S	S	P	S	S	G	S	S	P	S	S	G

(b)

G	S	P	S	G	S	P	S	G	S	P	S	G	S	P	S	G

(c)

G	P	S	G	P	S	G	P	S	G	P	S	G	P	S	G	P	S	G	P	S	G	P	S	G	P

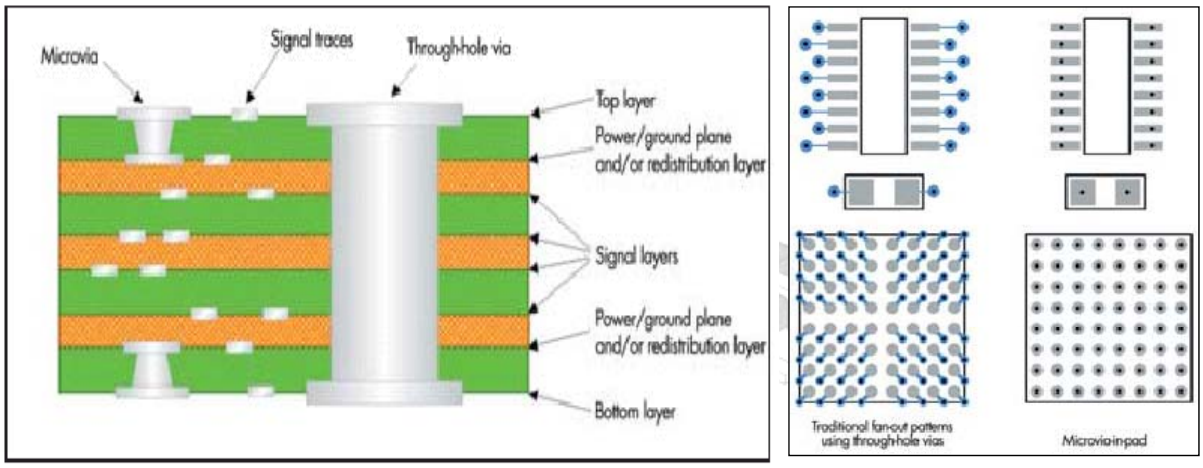
(d)

Eight-bit connector pin-out options assuming return current is flowing through both the power and ground pins: (*a*) inferior; (*b*) improved; (*c*) more improved; (*d*) optimal. G, ground pin; P, power pin; S, signal pin.

Rule of Thumbs For Connector

- Connector selection
  - Data sheets provide –3db loss bandwidth, x-talk figures and impedance value.
  - Select the –3db BW for at least > third harmonic of signal depending upon RISE time not BUS speed.
- Minimize the physical length of connector pins
- Maximize the ratio of power and GND pins to signal pins, if possible this ratio should be one.
- Place each signal pin as close as possible to current return pin.
- Place power pins adjacent to ground pins.

Via and Micro-via

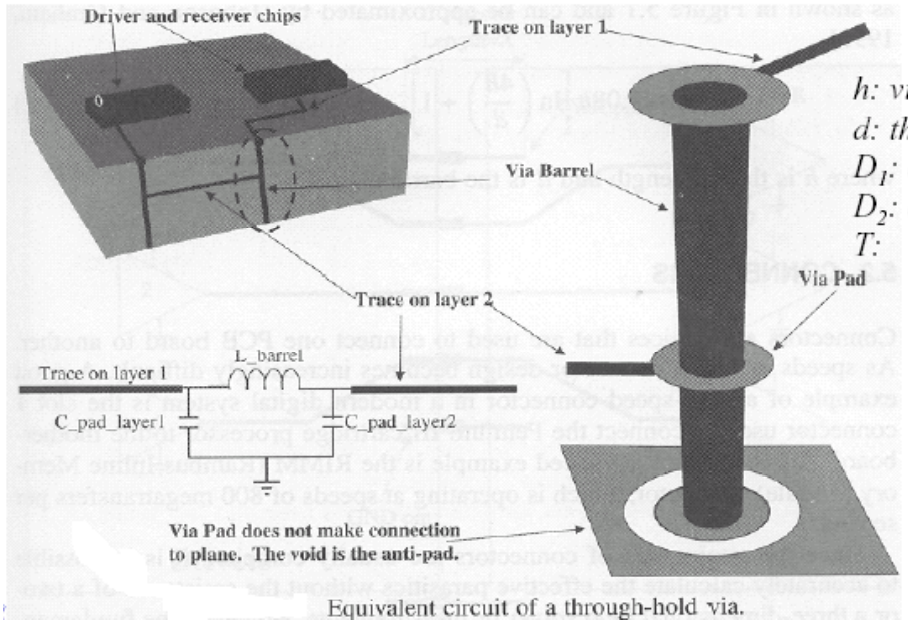


- Micro Via is blind via with diameter < 5 mil
  - Used in highly Dense boards inside pads with laser drilling
- Recommended for designs with 200 IO pins/sq in

Modeling of Through Hole Via

$$C_{via} \approx \frac{1.41\varepsilon_r D_1 T}{D_2 - D_1} \quad \text{picofarads}$$

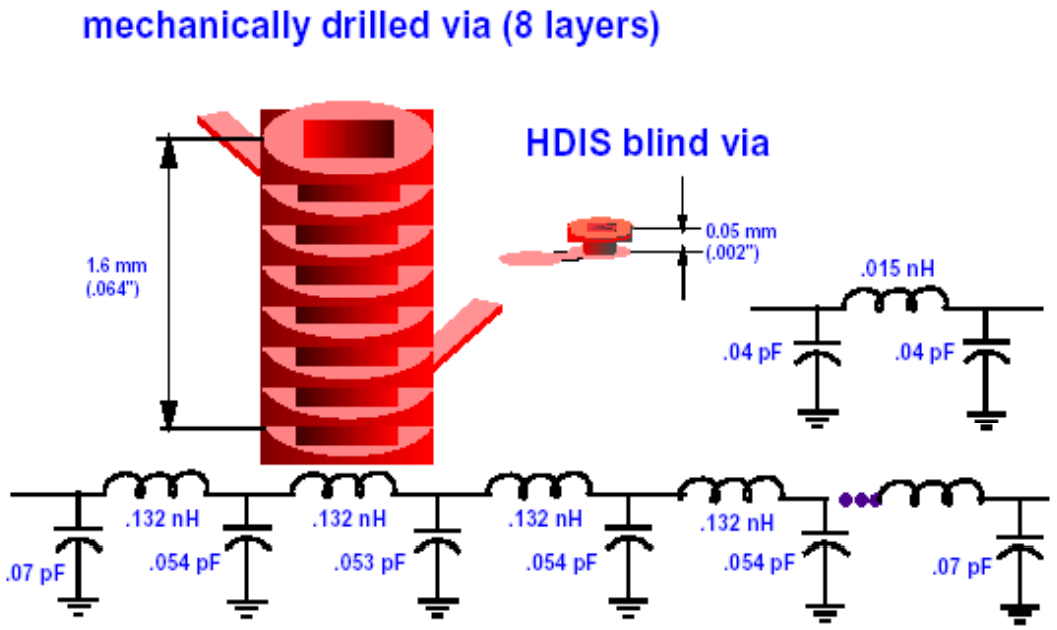
$$L_{via} \approx 2h\left[\ln\left(\frac{4h}{d}\right) + 1\right] \quad (nH)$$



Equivalent circuit of a through-hold via.

h: via length in cm
d: the barrier diameter
D_1: diameter of via pad
D_2: diameter of antipad
T:

Modeling of through Hole and Blind HDI Via



Standard Via Sizes

Table 1 – Standard hole sizes for a typical fabricator

	Standard	Engineering
Minimum Finished Hole Size	0.008"	0.006"
Minimum Drill Size	0.01"	0.008"
Minimum Required Pad	Drill size + 0.014"	Drill size + 0.010"
Resulting Annular Ring	0.001"	Tangency
Minimum Drill to Plane Clearance	0.012"	0.009"
Minimum Drill to Trace (Internal)	0.01"	0.009"
Maximum Apect Ratio	10:1	14:1

Table 2 – Laser drilling capabilities of an advanced PCB facility

	Standard	Engineering
Minimum Finished Hole Size	0.002"	0.001"
Minimum Drill Size	0.006"	0.004"
Minimum Required Pad	0.012"	0.008"
Resulting Annular Ring	Tangency	Tangency
Minimum Drill to Plane Clearance	0.01"	0.008"
Minimum Drill to Trace (Internal)	0.01"	0.008"
Apect Ratio	1:1	1:1

Via: Aspect ratio and Tear Drops

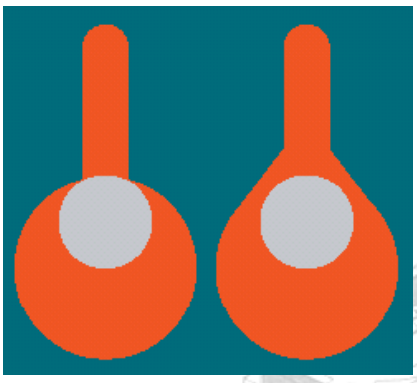
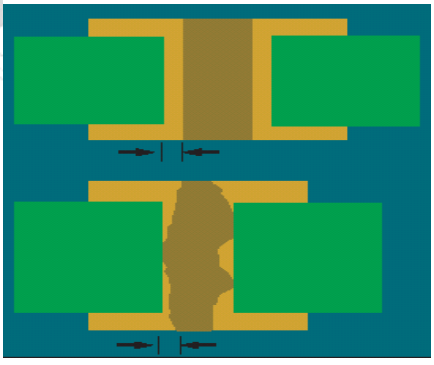


Figure 1 – A pad with (right) and without (left) a teardrop. Teardropping provides a strong hole-to-trace connection

Figure 2 – A pad with a good aspect ratio (at top) is characterized by a hole diameter in proportion to the hole depth, which facilitates uniform plating. A hole that is too narrow or deep (bottom) is harder to plate



Summary

- Why is packaging important ?
  - Trends in packaging
  - Impact on high speed signals
  - Package and connector models
  - IC packages
    - Through hole
    - Surface mount
  - Connectors
    - Surface mount
    - Through hole
- Via and Via Types
  - Via Modeling
  - Standard Sizes, HDI

Wakeup Please lets have Some Food....