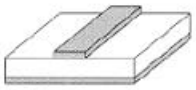
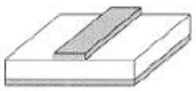


Signal Driver/Receiver IBIS Models and Assembly Techniques

Rashad.M.Ramzan, Ph.D

FAST-NU, Islamabad



Today's Topics

- Signal Buffer Driver and receiver
  - Standards, CMOS Buffer, Driver, Receiver
  - CMOS Buffer (Tapered)
  - Differential CMOS Driver and Receivers
- IBIS Models
  - Definition
  - Basic Components of IBIS Model
  - Validation and Quality Assurance
- Assembly Techniques
  - THD, Wave Soldering
  - SMD, Reflow Soldering
  - Types of reflow Soldering

Common Standards

Comparison of driver specifications for several common signaling standards.

Standard	V_{DDQ}, V	V_{OL}, V		V_{OH}, V		$V_{differential}$, V		V_{offset}, V		Termination	Driver[a]
		Min	Max	Min	Max	Min	Max	Min	Max		
TTL	$5 \pm 10\%$		0.4	2.4						None	PP
LVTTL[b]	$3.3 \pm 10\%$		0.4	2.4						None	PP
GTL[c]	$1.2 \pm 5\%$		0.4	V_{DDQ}-0.4	V_{DDQ}					None	PP
GTL			0.4							R to $1.2 \pm 5\%$ V[d]	OD
HSTL[e]	1.5 ± 0.1		0.4	$V_{DDQ} - 0.4$						[f]	PP
ECL[g]	$-5.2 \mp 5\%$	-1.810	-1.620	-1.025	-0.880					50Ω to -2V	CM
PECL[h]	$5.0 \pm 5\%$	3.190	3.380	3.975	4.120					50Ω	CM
LVPECL[i]	$3.3 \pm 5\%$	1.490	1.680	2.275	2.420					50Ω	CM
LVDS[j]		0.925			1.474	0.250	0.400	1.125	1.275	50Ω	CM

a. PP - push-pull; OD - open-drain (active pull-down); CM - current-mode

b. JEDEC Standard, "Interface standard for nominal 3V/3.3V supply digital integrated circuits," Electronic Industries Association, JESD8-A, June 1994.

c. JEDEC Standard, "Gunning transceiver logic (GTL) low-level, high-speed interface standard for digital integrated circuits," Electronic Industries Association, JESD8-3. The standard defines unterminated and terminated implementations. GTL is patented.

d. The resistor value is chosen to match the impedance of the system.

e. EIA/JEDEC Standard, "High-speed transceiver logic (HSTL) a 1.5V output buffer supply voltage-based interface standard for digital integrated circuits," Electronic Industries Association, EIA/JEDEC8-6, August 1995.

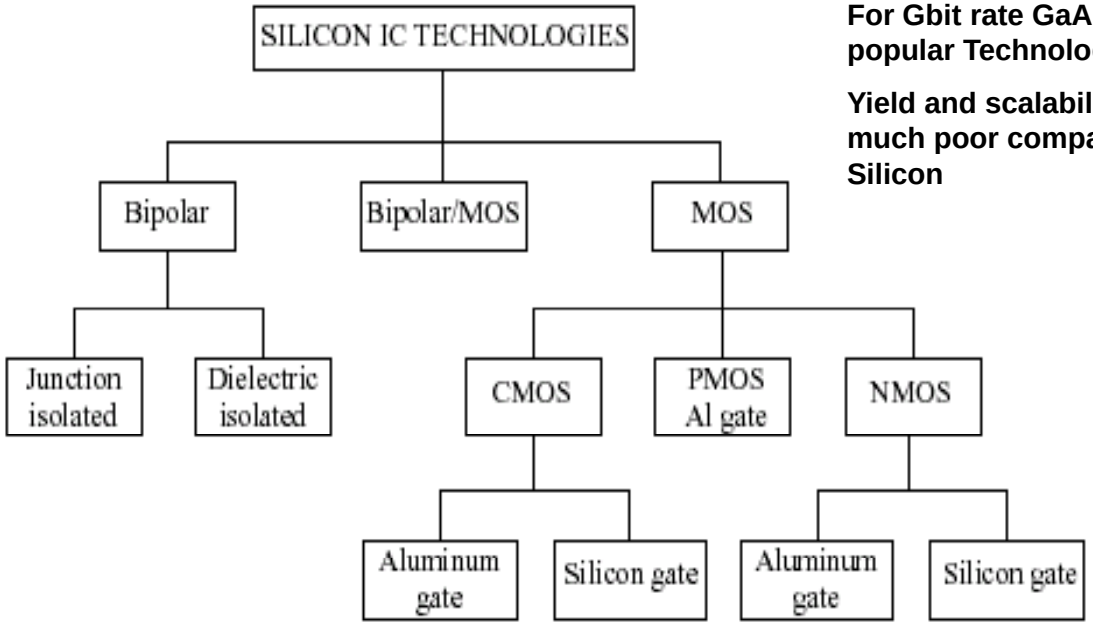
f. HSTL defines driver types I–IV for four cases of unterminated, source terminated, far-end terminated, and far-end plus near-end parallel terminated, respectively. All must satisfy the same output specifications.

g. JEDEC Standard, "Standard for operating voltages and interface levels for low voltage emitter-coupled logic (ECL) integrated circuits," Electronic Industries Association, JESD8-2, March 1993.

h. PECL (Positive ECL) is ECL run with a +5V supply. See Cleon Petty and Todd Pearson, "Designing with PECL (ECL at +5.0V)," Motorola Application Note AN1406, Feb. 1998.

i. LVPECL (Low-Voltage PECL) is ECL run with a +3.3V supply.

Types of Si IC technology

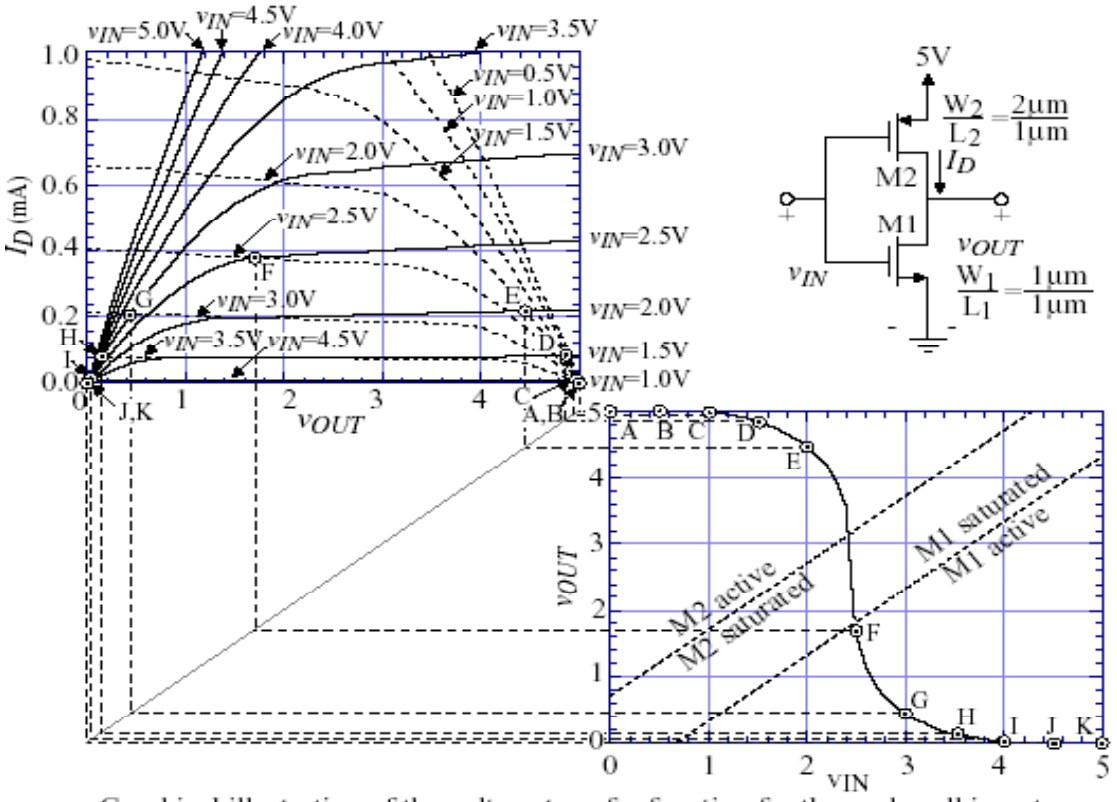


For Gbit rate GaAs is popular Technology

Yield and scalability is much poor compared to Silicon

Silicon Gate CMOS is technology of Choice today for +90% digital Circuits.

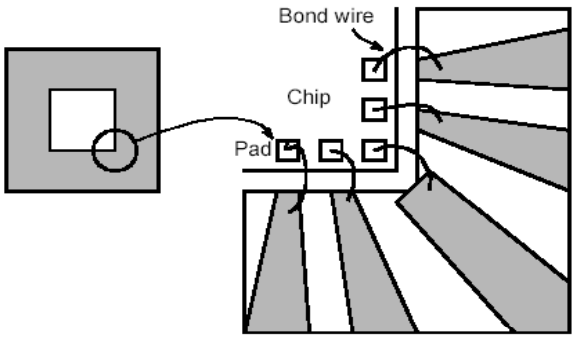
CMOS Buffer Drivers (Inverter)

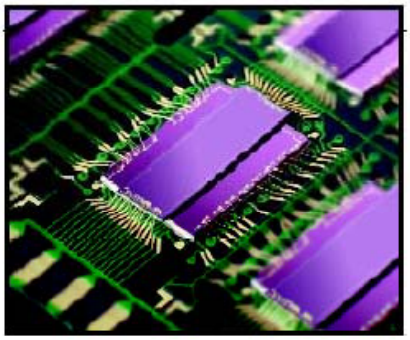


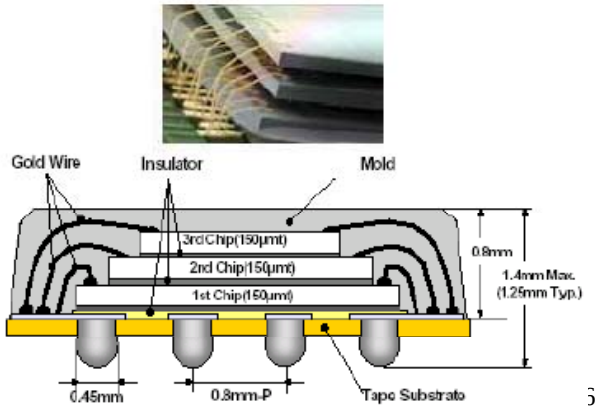
Graphical illustration of the voltage transfer function for the push-pull inverter.

Load Buffer has to Drive

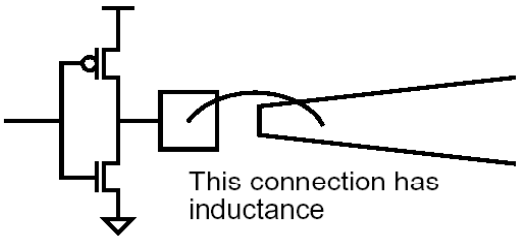
- Must be able to drive heavy capacitance.
- Must have very Low output impedance.





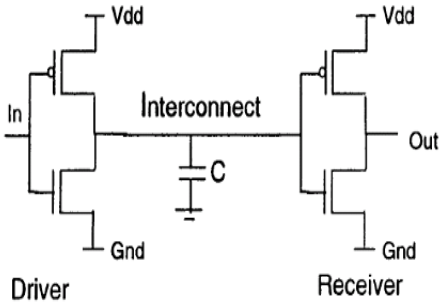


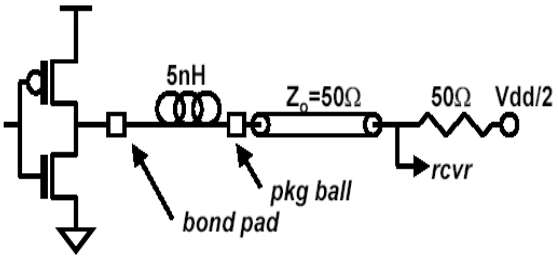
Load Buffer has to Drive



Bond wire is ~ 1nH/mm (2mm long)

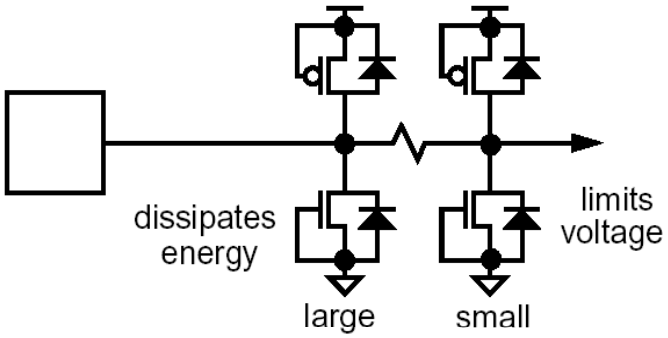
Package is ~ 3-10nH

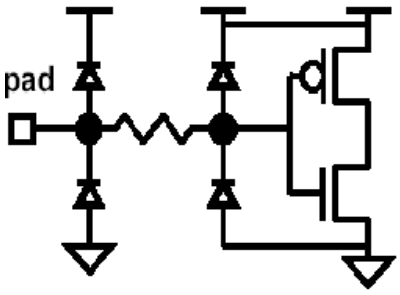




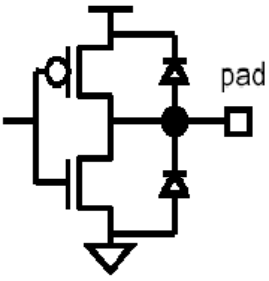
- $L = L_{Bondpad} + L_{Drv.PackagePin} + L_{interconnect} + L_{RcvPackagePin} + L_{Rcv.PackagePin}$
- $C = C_{Bondpad} + C_{Drv.PackagePin} + C_{interconnect} + C_{RcvPackagePin} + C_{Rcv.PackagePin}$
- The typical inductance is 10-50nH
- The Typical capacitance ~500pF

IO Buffers and ESD

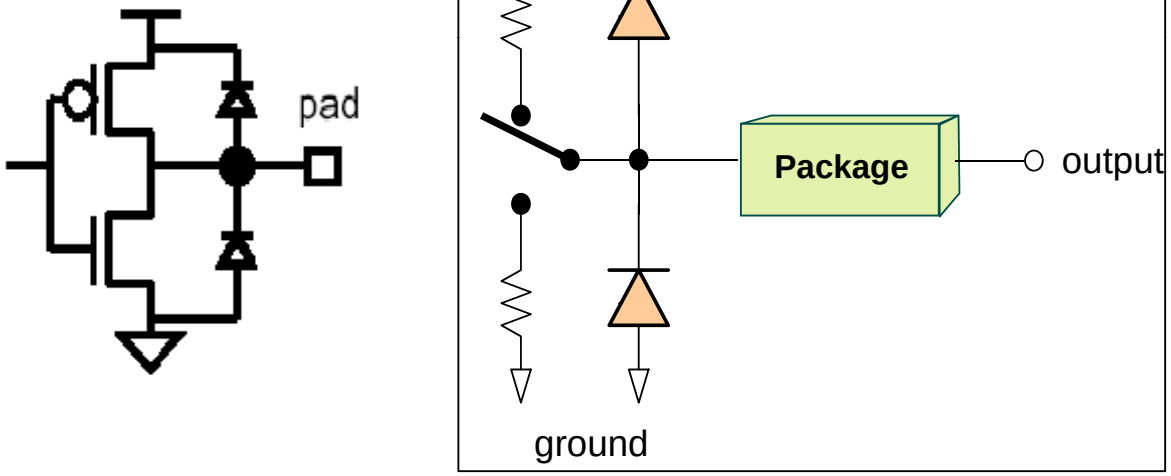




- This is simplified diagram
- Actual ESD protection is much more complex and designed by foundries with pad provided in libraries.
- **The protection adds up to the load of Drivers. The diodes are very wide and have lot of on-chip non-linear capacitance.**



CMOS Inverter

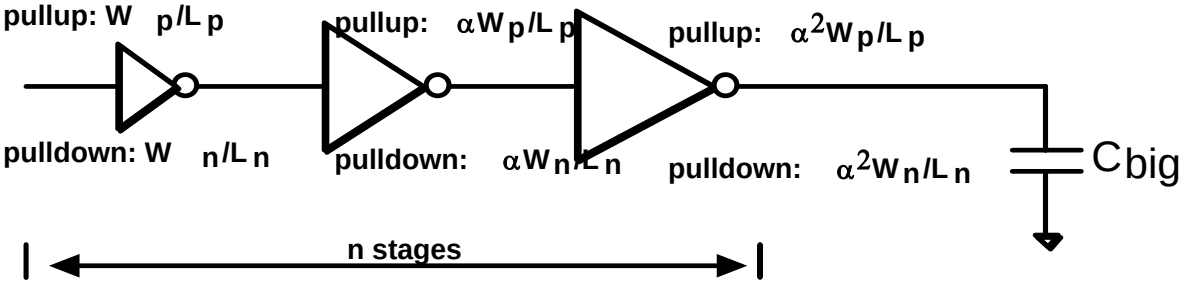


Limitation of Single Ended Output Buffer

- Single stage can not drive the out of Chip capacitance.
- Solution : Progressive increase in Size, stages of progressively larger transistors

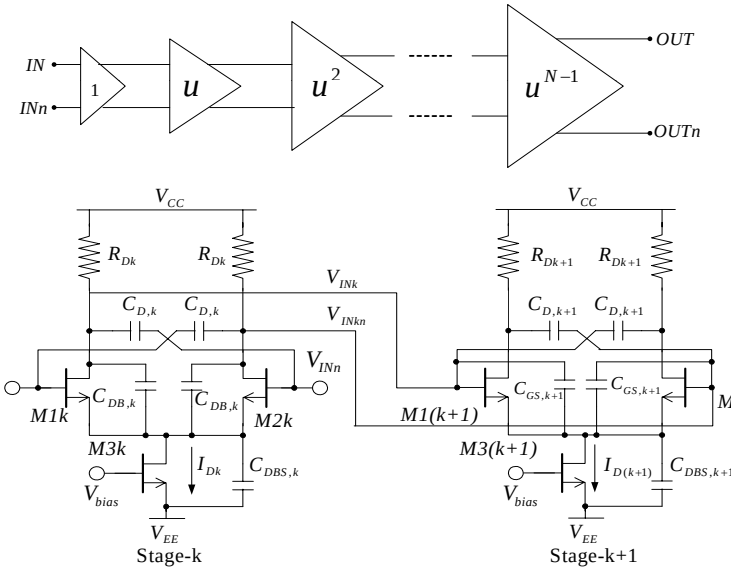
Use $n_{opt} = ln(C_{big}/C_g)$.

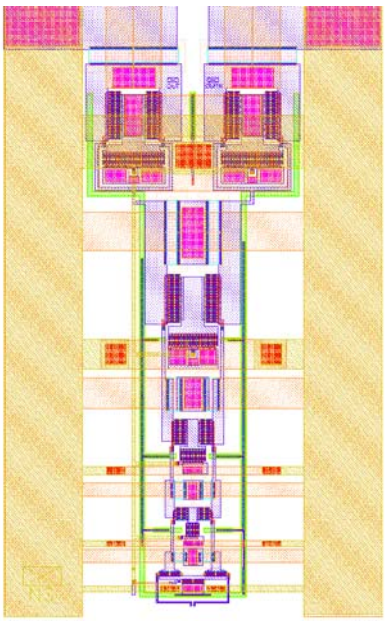
Scale by a factor of $\alpha = e$ (gives best results)



My Design: Differential O/P Buffer

- MCML Buffer to Drive 50 Ω load (1.5 GHz)
- 0.35um CMOS Technology

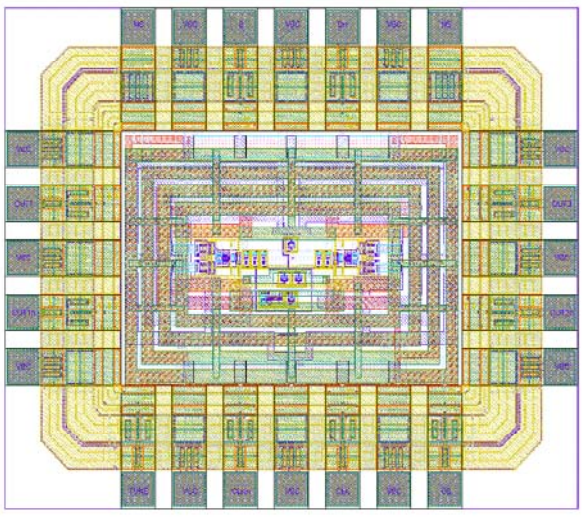


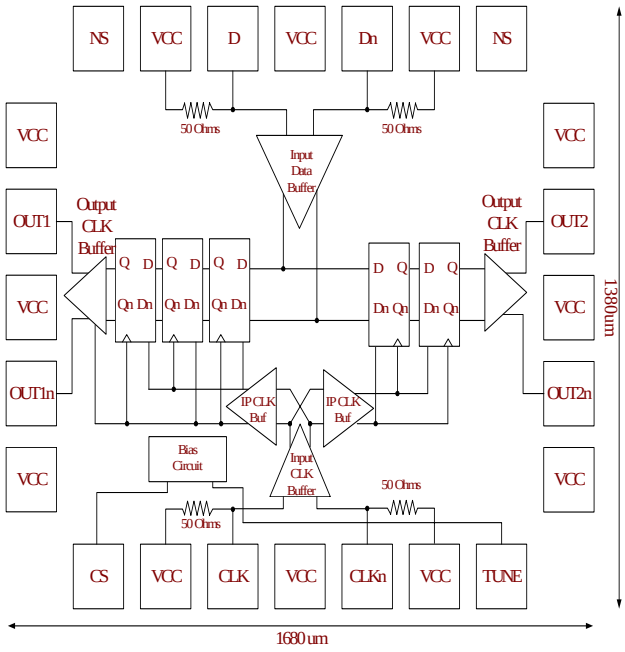


©Fraunhofer IIS Germany

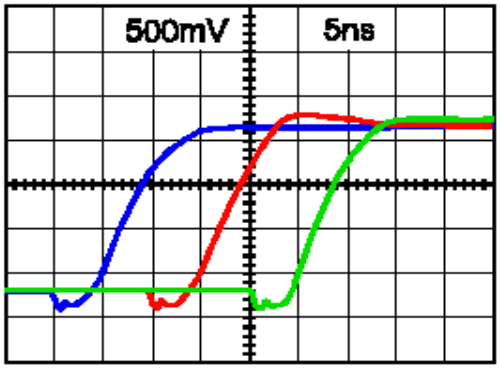
My Design: 2:1 DEMUX

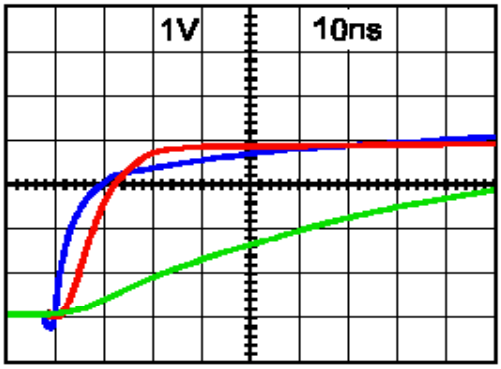
- 2:1 MCML DEMUX (1.6 GHz)
- 0.35um CMOS Technology

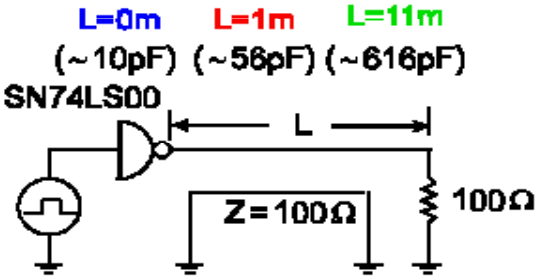


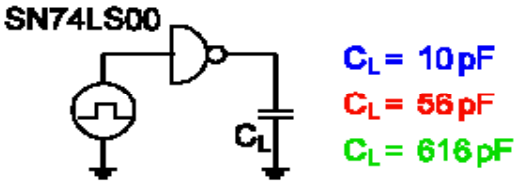


Limitation of Single Ended Output Buffer



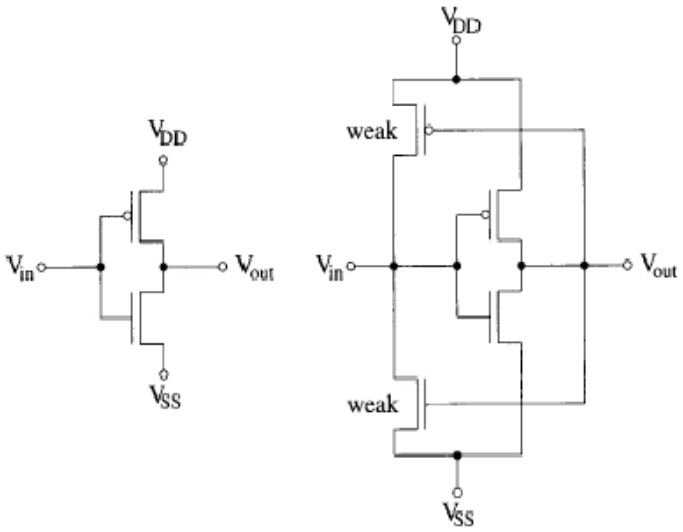






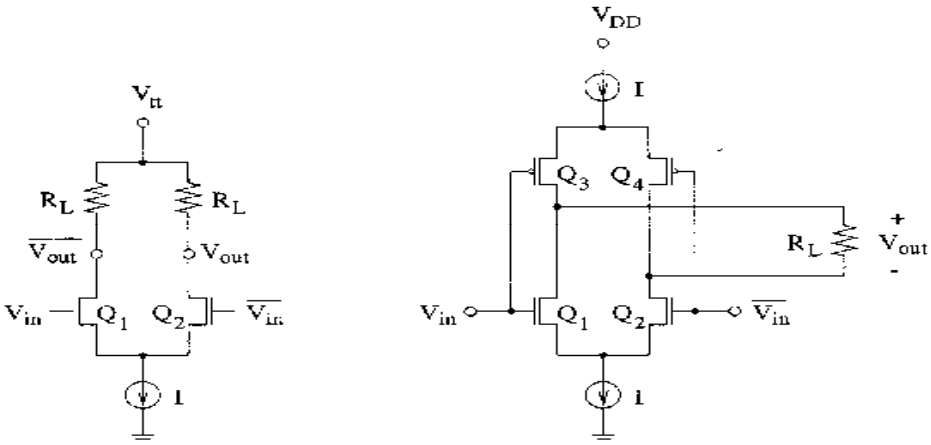
CMOS Single-ended Receivers

When input buffer has to drive many loads on the chip like CLK the Multi-stage technique is also used in input buffer.



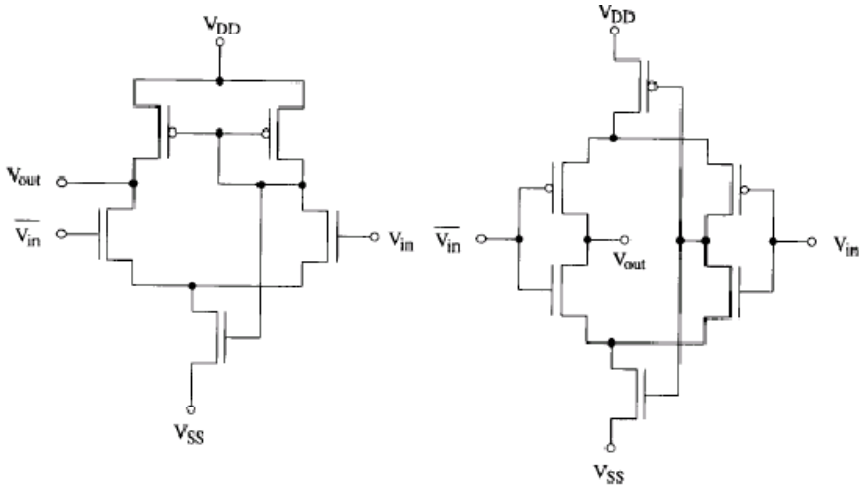
CMOS inverter-based single-ended receivers: (a) simple inverter, (b) inverter with feedback.

Differential Signal Driver and Receiver



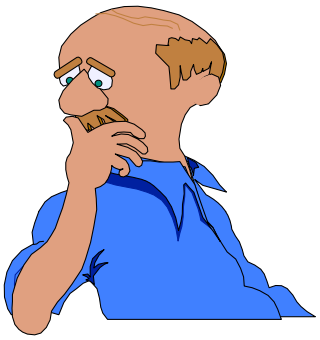
- Uses two transmission lines
- Voltage measured between the transmission lines
- Voltage Swing +/- IR_L
- Parallel termination or Source termination used
- Keep power supply noise to a minimum
- Ideally suited for high data rates

CMOS Differential Receivers



Two circuit topologies for implementing differential receivers.

IBIS Models



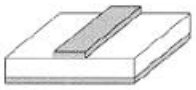
- What is IBIS?
- There are two choices:
  - Find and use an existing model
  - This option is your least expensive choice by far
- Create a new model

– The second option will be briefly explained because

  - You might need it!!
  - You need to understand making a model when you're going to encounter multiple mistakes to correct.

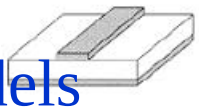
IBIS History

- IBISver 1.0 ; Released April 1993
- IBISver 1.1 ; Released June 1993 at DAC, Dallas
- IBISver 2.0 ; Ratified June 1994 at DAC, San Diego
- IBISver 2.1; ANSI/EIA-656 Approved Dec. 1995
- IBISver 3.0 ; Ratified June 1997 at DAC, Los Angeles
- IBISver 3.1 ; Editorial changes implemented.
- IBISver3.2; ANSI/EIA-656-A ratified Sept 1999.
- IBISver4.0; IBIS version 4.0 ratified July 2002 by the IBIS OF
- IBISver4.1; IBIS version 4.1 ratified February 2004 by the IBIS OF
- IBISver4.2; IBIS version 4.2 ratified June 2006 by the IBIS OF
- IBISver5.0; IBIS version 5.0 ratified Aug 2008 by the IBIS OF



IBIS Models

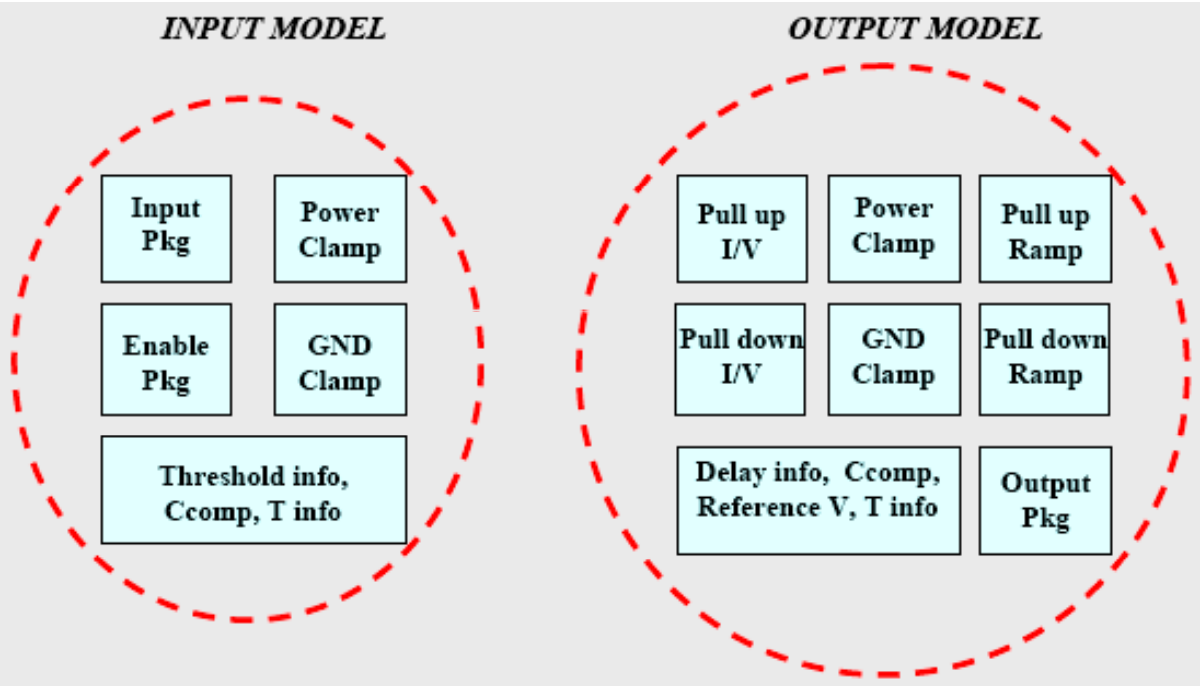
- Earlier Modeling Techniques
  - Like SPICE use the actual designs and reveal sensitive information about buffer design and underlying fabrication technology.
  - SPICE based models are SLOW.
- Solution is IBIS models
  - **IBIS**: IO Buffer Information Specification
  - Available from most IC vendors
- http://www.eigroup.org



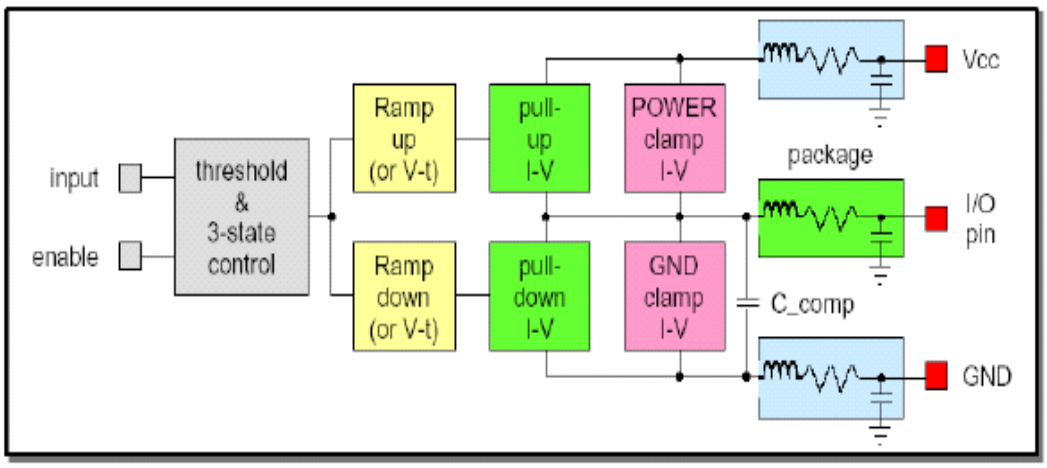
Finding and Using Existing IBIS Models

- The web - start at:
  - http://www.vhdl.org/ibis/
  - http://www.freelists.org/archives/si-list
  - http://www.qsl.net/wb6tpu
  - http://www.freelists.org/webpage/si-list
- Vander (Portal, cadence) libraries
- The supplier
- The SI reflector
- Similar Parts 3rd party custom
- Usage: Depends upon Simulator

Blocks for Simple IO Buffer

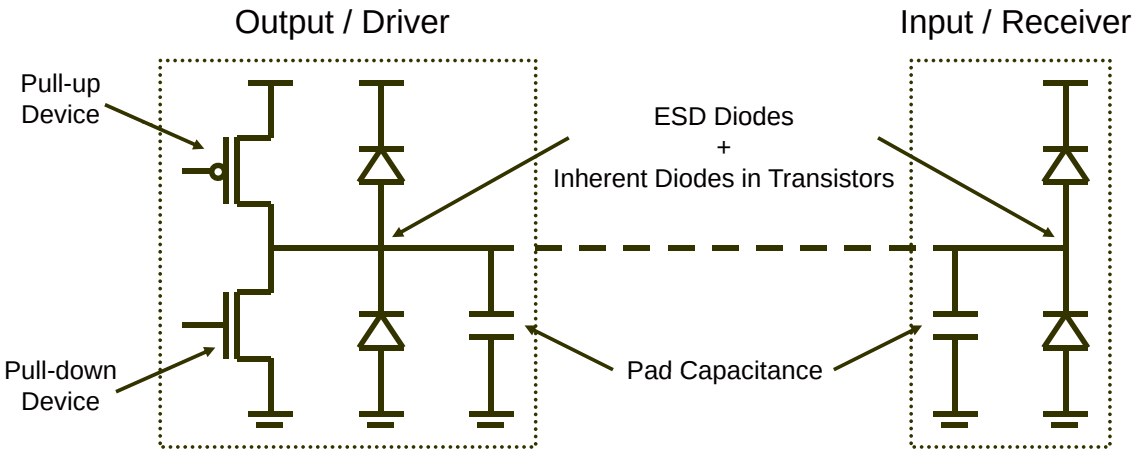


Basic Building Block of IBIS Model



Block diagram of CMOS buffer

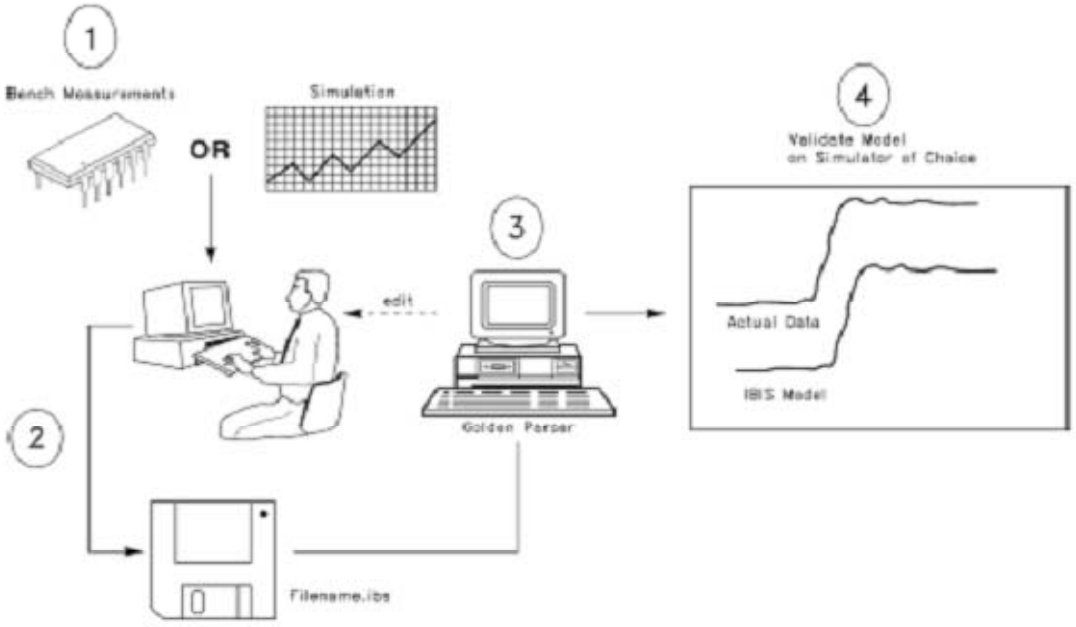
Basic CMOS Buffer Model



Parts of Basic IBIS Model

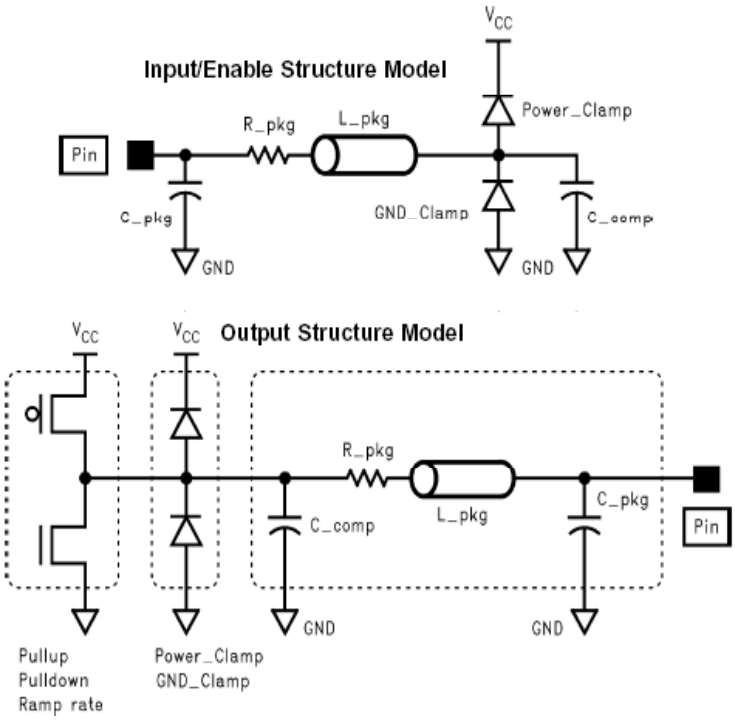
- Four I-V Curve
  - Pull-up and Power Clamp
  - Pull-down and GND Clamp
- Two Ramps
  - dv/dt rise
  - dv/dt fall
- Die Parasitic
  - Capacitance; c_comp
- Package Parasitic
  - Capacitance
  - Resistance
  - Inductance

IBIS Model Generation Flow



IBIS Model Generation Flow

Input and Output Buffer

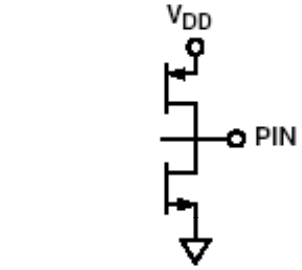


The output model is characterized by the following dc electrical data, ac or switching data, and parameters:

1. Pull-Up and Pull-Down Curves
2. Power and GND Clamp Curves
3. Ramp Rate
4. Rising and Falling Waveforms
5. C_Comp
6. Package Parameters

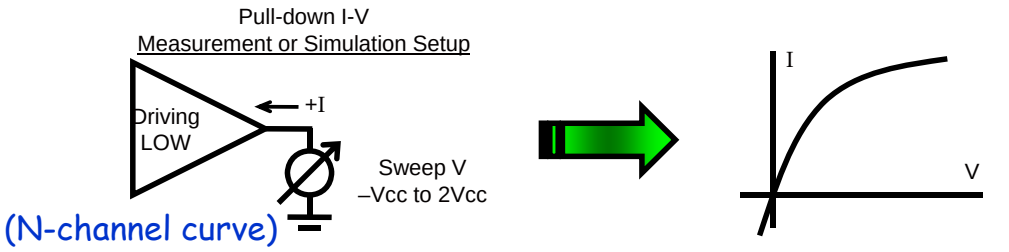
Pull-up & Pull-down Data

- Define drive strength of the device.
- Obtained by characterizing the two transistors in the output
- Pull-up data describes the I/V behavior when the output is logic high (PMOS off).
- Pull down data shows the when the output is in a logic low state (NMOS transistor.
- Data needs to be acquired from - V_{DD} to 2 V_{DD}. range covers the region where undershoot, overshoot, and reflections in the transmission line could happen.

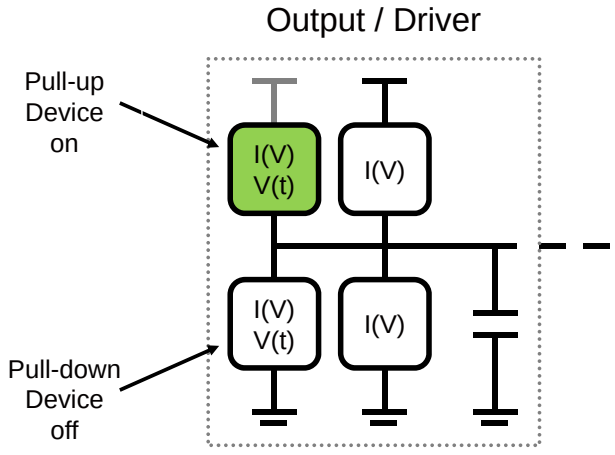



```
[Pulldown                    I/V PULLDOWN DATA
-----------
-3.60000V    -373.560uA
-3.30000V    -373.560uA
-3.00000V    -373.560uA
0.00000V     -373.560uA
...          ...
6.00000V      29.8895mA
6.60000V      30.0423mA
7.20000V      30.1951mA
|
```


Generating Pull-Down I-V Data



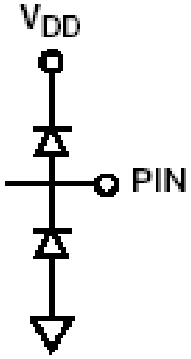
(N-channel curve)



Current is positive above Vss per definition if I flows

Power and GND Clamp Curves

- These curves are generated when the output is in a high impedance state.
- The GND and power clamp data represent the electrical behavior of the output when the GND clamp and the power clamp diodes are turned on, respectively.
- The GND clamp is active when the output is below ground, and the power clamp is active when the output is above VDD
- Data needs to be acquired from $-V_{DD}$ to V_{DD} GND and V_{DD} to V_{DD} for PWR clamp.
-



Ramp and Switching Waveforms

- The ramp rate (dV/dt) describes the transition time when the output is switching from the current logic state to another logic state. It is measured at the 20% and 80% points with a default resistive load of 50 Ω.
- For a standard push/pull CMOS, four different waveforms can be generated: two rising and two falling. Load connected to V_{DD} and the other with the load connected to GND.

```
[Falling Waveform]   <-- SWITCHING WAVEFORMS
R_fixture = 50.0000
V_fixture = 0.00000
|
0.00000s   1.04159V          NA     NA
560.000ps  1.03353V          NA     NA
...          ...             ...    ...
6.60000ns  15.5525mV         NA     NA
9.98000ns  11.3165mV         NA     NA
|
[Ramp]   <-- RAMP RATE
| variable typ min max
dV/dt_r 613.749m/1.89595n    NA     NA
dV/dt_f 841.756m/1.65434n    NA     NA
R_load = 50.0000hms
|
[End]
```

C_Comp and Package RLC

TIMING TEST LOADS AND DIE CAPACITANCE

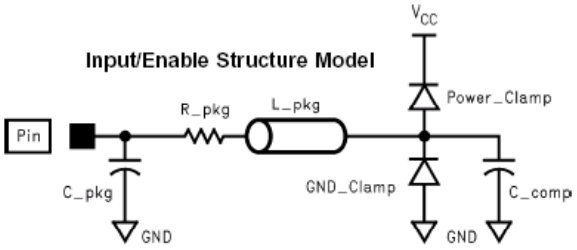
```
Vref=1.50000V
Rref=50.0000ohms
Cref=2.00000pF
Vmeas=1.50000V
C_comp 3.00000pF 3.00000pF 3.00000pF
```

```
[Package]
| variable   typ    min    max
R_pkg  0.010ohms 0.009ohms 0.011ohms
L_pkg  1.933nH   1.900nH   1.966nH
C_pkg  1.000pF   0.900pF   1.100pF
```

PACKAGE PARAMETERS

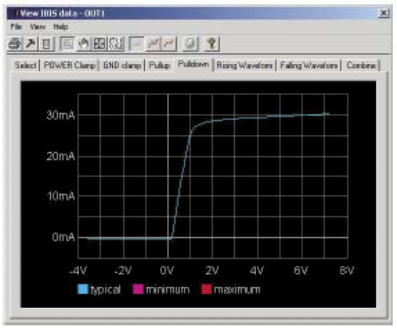
```
[Pin] signal_name  model_name  R_pin  L_pin C_pin
1       DVCC     POWER    0.01    3.71E-09        1.23E-12
...     ...      ...      ...          ...              ...
33      DVCC     POWER    0.01    3.03E-09        1.00E-12
51      D13      OUT1     0.01    3.71E-09        1.23E-12
52      DRY      OUT3     0.01    3.95E-09        1.31E-12
```

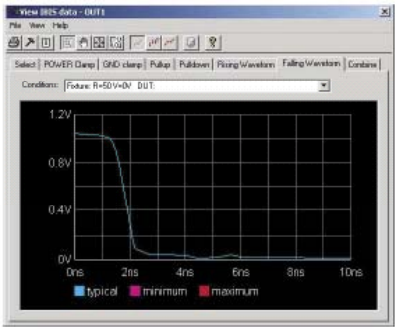
ASSIGNED PIN MODEL



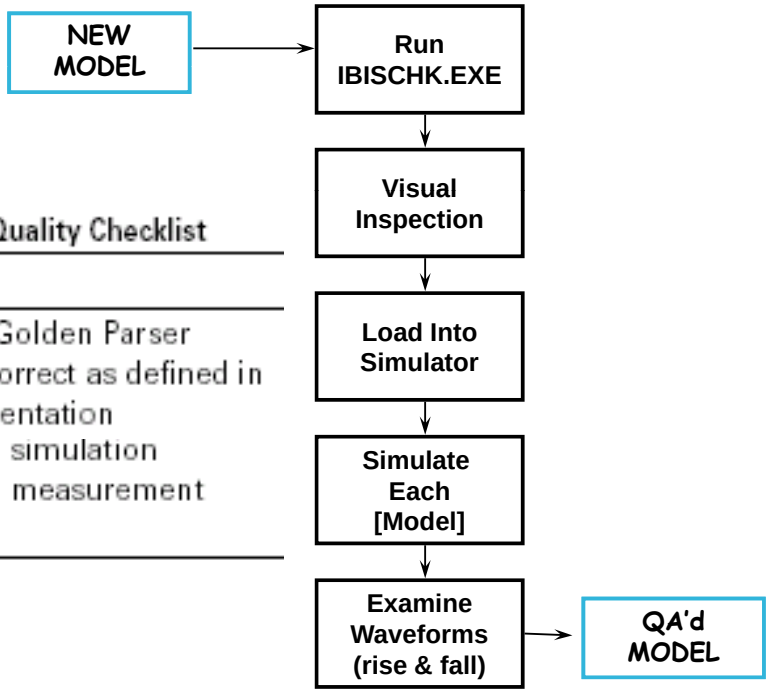
Model Validation

- IBIS file is validated using Golden Parser, also known as ibischk3.
- Checks to ensure the syntax and structure of the file complies with the IBIS specification.
- Available at http://www.eigroup.org/ibis/tools.htm
- Next, the user should make a visual inspection of the I/V and V/T curves generated from the file and make sure that the results are as expected. This can be done using a Visual IBIS Editor from Innoveda, available at the IBIS website at no charge.
- Last step is to compare the results with SPICE measurement and finally with Silicon measurement.





Quality Level of IBIS Model



Quality Levels in the IBIS Quality Checklist

Quality Level	Description
Level 0	Passes ibischk, Golden Parser
Level 1	Complete and correct as defined in checklist documentation
Level 2a	Correlation with simulation
Level 2b	Correlation with measurement
Level 3	All of the above

Data Required for IBIS Model - Preamble

Keyword	Description	Where to Get?				Notes
		ds	sp	ms	lg	
[IBIS Ver]	Version of IBIS Syntax used in file	-	-	-	-	Don't confuse with [File Rev]
[File Name]	Name of the model file	-	-	-	-	Must end in .ibs
[File Rev]	Revision of the model file	-	-	-		Numbers have meaning (e.g., 2.x means correlated)
[Component]	Name of the component modeled	1				
[Manufacturer]	Manufacturer of the component	1				Even second sources might have unique models
[Package]	Global Packaging Parameters	2	3	4	1	Default R_pkg, L_pkg, C_pkg to use on all comp. pins
[Pin]	Pinout of the component	1				Maps pin# to signal_name to model type (opt. pin RLC)

Preamble, up to I/O [model]s - lists most common sources of information: ds=datasheet, sp=spice, ms=measurement, lg=legacy, borrowed from similar device models

Data Required for IBIS Model - MODELS

Required, only if they exist in device

Keyword	Description	Where to Get?				Notes
		ds	sp	ms	lg	
[Model]	One of the comp-onent's I/O Models	-	-	-	-	Marks the beginning of the I/O's full description
Model_type	Type of I/O cell: Input, 3-state, etc	1	2			[Model] sub-parameter, 16 defined types
C_comp	Die capacitance of I/O cell	1	3	3	2	[Model] sub-parameter, often inaccurate
[Voltage Range]	Specified operating range on I/O cell	1				Vcc, with tolerances
[Pulldown]	Low-state Driver V/I Curve	3	1	2	4	Must include at least typical data
[Pullup]	High-state Driver V/I Curve	3	1	2	4	Data listed is "Vcc Relative" not ref. to GND
[GND Clamp]	V/I Curve of ESD (Diode) structure	3	1	2	4	Clamping characteristics below ground
[POWER Clamp]	V/I Curve of ESD (Diode) structure	3	1	2	4	Clamping characteristics above Vcc
[Ramp]	Edge Rate of [Pulldown]/[Pullup]	2	1	3	4	Expressed as 20%-80% dv/dt into 50 Ohms to Vcc or GND
[End]	End of the file	-	-	-	-	That's all!

IBIS Models normally have numerous [Model]s, most common source of data: ds=datasheet, sp=spice, ms=measurement, lg=legacy

IBIS Text Style

[Pull-down]

Voltage	I(typ)	I(min)	I(max)
-5	-177.7m	-165.8m	-189.6m
-4	-149.5m	-138.8m	-160.1m
-3	-117.5m	-108.5m	-126.5m
-2	-81.4m	-74.5m	-88.3m
data omitted			
10	139.4m	128.6m	150.2m

[Pull-up]

Voltage	I(typ)	I(min)	I(max)
-5	-223.0m	-204.0m	-242.0m
-4	-197.4m	-190.7m	-204.0m
-3	-161.8m	-156.6m	-167.0m
-2	-125.3m	-118.6m	-132.0m
data omitted.			
10	0.0	0.0	0.0

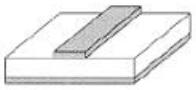
[GND_clamp]

Voltage	I(typ)	I(min)	I(max)
-5	-188.3m	NA	NA
-4	-144.9m	NA	NA
-3	-109.3m	NA	NA
-2	-58.9m	NA	NA
data omitted.			

[POWER_clamp]

Voltage	I(typ)	I(min)	I(max)
-5	18.4m	NA	NA
-4	11.6m	NA	NA
-3	3.5m	NA	NA
-2	0.8m	NA	NA
data omitted.			
10	0.1u	NA	NA

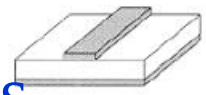
IBIS Text Style



```
[Ramp]
|              typ              min              max
dV/dt_f      1.98/58p  1.87/60.5p  2.09/56.9p
dV/dt_r      1.55/158p 1.46/160p   1.64/177p
```

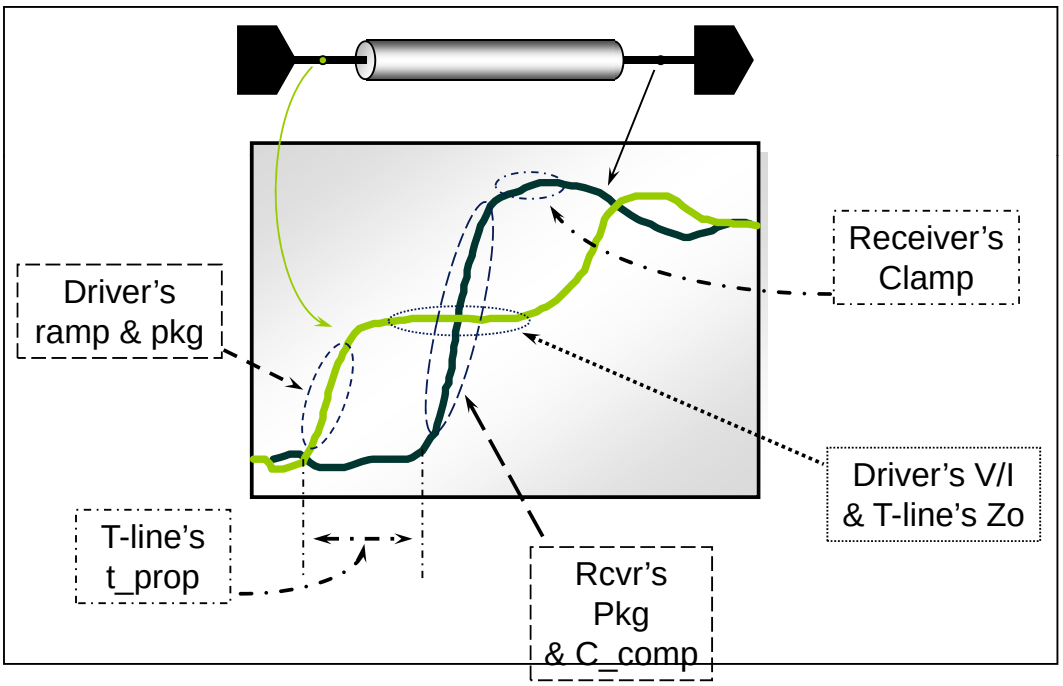
```
[Package]
|
|              typ              min              max
R_pkg        52mohm           51mohm           53mohm
L_pkg        6.425nH          3.33nH           9.52nH
C_pkg        0.875pF          0.4pF            1.35pF
•
data omitted. . . . .
•
|              typ              min              max
C_comp       2.33p            2.17p            3.14p
```


Gathering Data From Datasheets



- All datasheets have:
  - component name, manufacturer, pinout, vinl, vinh, voltage range
- Most datasheets have:
  - model_type, testloads, c_comp
- Few datasheets have:
  - vi curves, ramp rates, package RLC
- No datasheets have:
  - pin (power bus) mapping, v/t curves
- However, good interface specifications have it all!

Correlating Waveforms

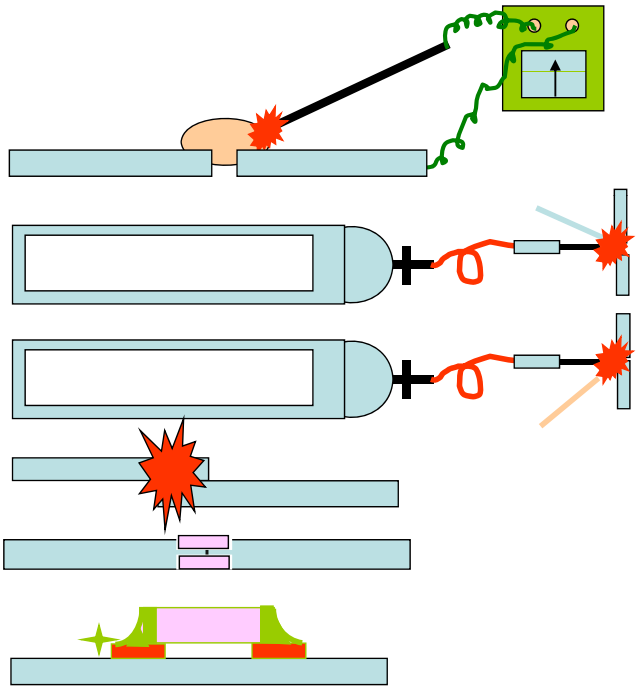


Assembly Techniques

Through Hole Devices (THD)
and
Surface Mount Devices (SM)

Joining Methods in Electronics

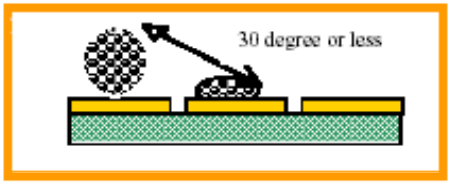
- Electric Welding
- Gas Welding
- Brazing
- Friction Welding
- Cold Welding
- Soldering



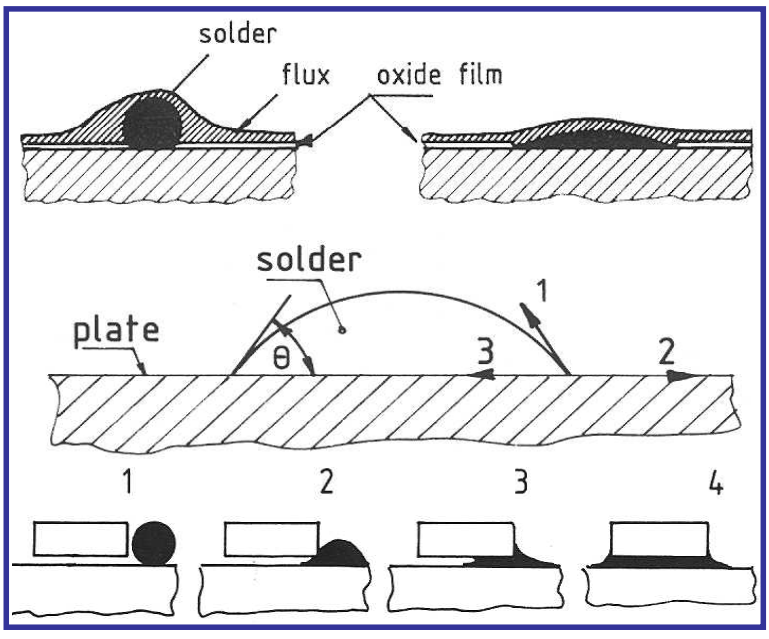
Soldering Principle

Types of Soldering

- **Hand Soldering**
- **Drag Soldering**
- **Wave Soldering**
- **Reflow Soldering**

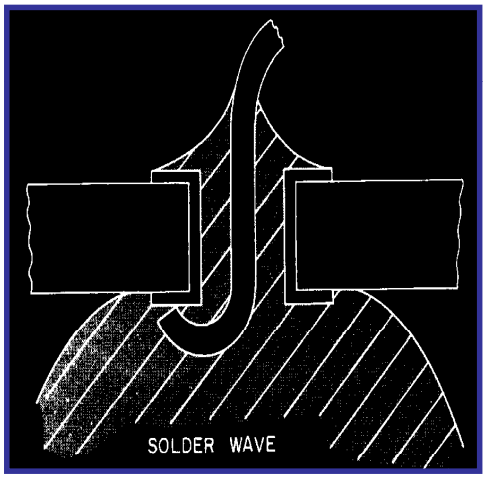


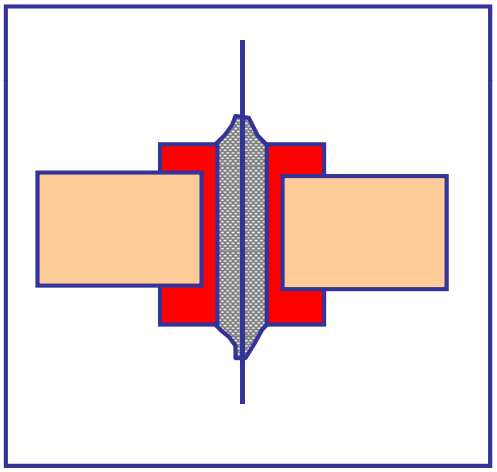
Concept of contact angle and wetability



Soldering Principle

Solder wicking due to surface tension



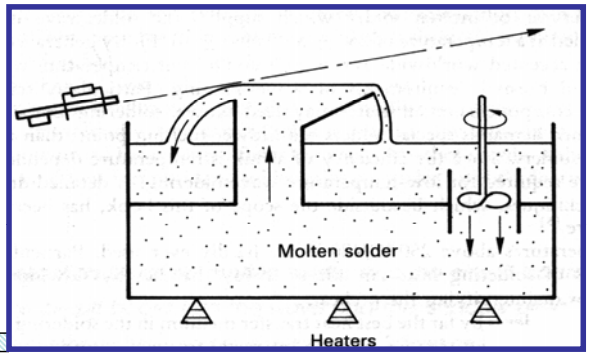


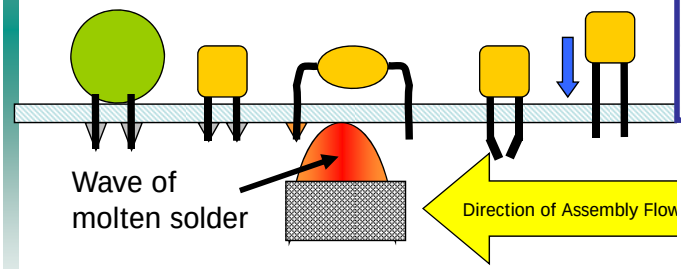
Electronics Assembly

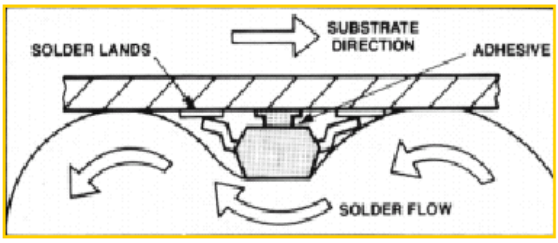
- Soldering Principles
- THD Assembly
  - Component Insertion (Hand or Auto Insertion)
  - Hand Soldering or Wave Soldering
- SMD assembly
  - Solder paste Application
  - Adhesive Application
  - Placing the Parts
  - Reflow Soldering

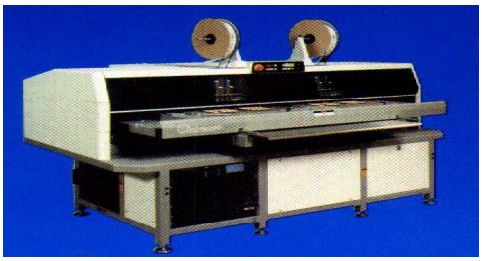
THD Assembly -Wave Soldering

1. **Leaded parts are inserted into holes in circuit board**
2. **Leads are clinched and cut.**
3. **Molten wave of solder connects leads to board**



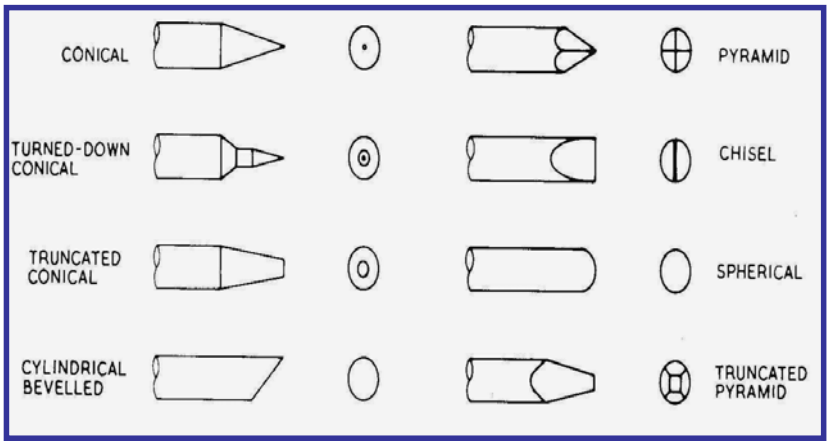






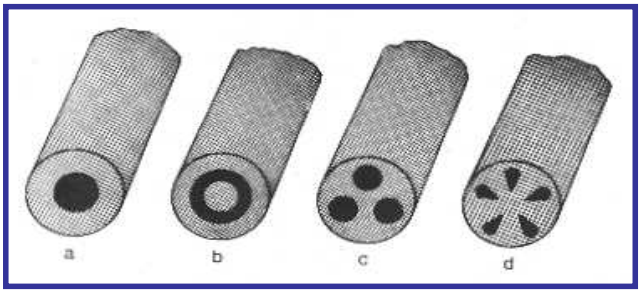
Incase of SMD the whole part has to submersed in solder. Adhesive is required to keep the component in place

THD Assembly -Hand Soldering

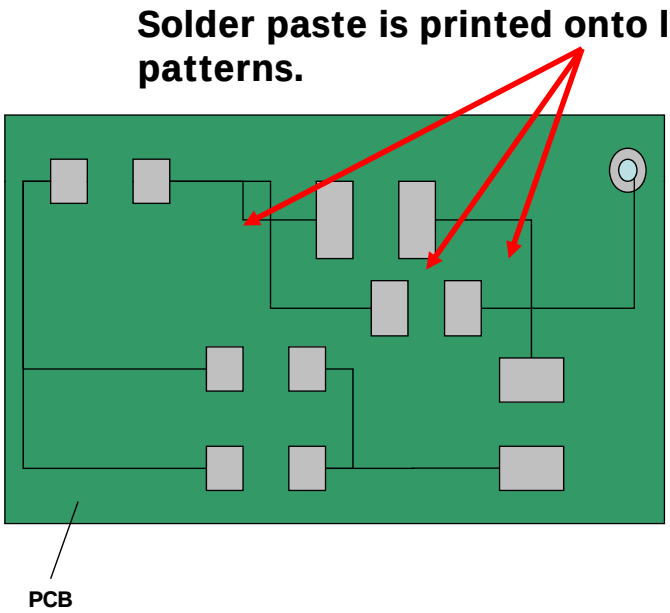


Solder bit Shapes

Flux Cored Solder Wire

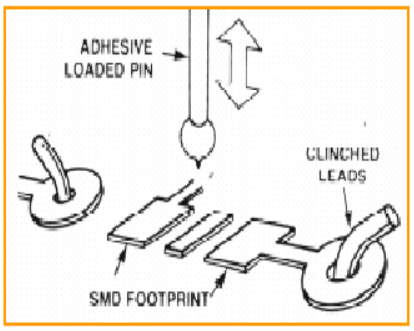


SMD Assembly- Solder paste Application



- Pin Transfer
- Pressure Syringe
- Screen Transfer
- Stencil Transfer

SMD Assembly- Adhesive Application

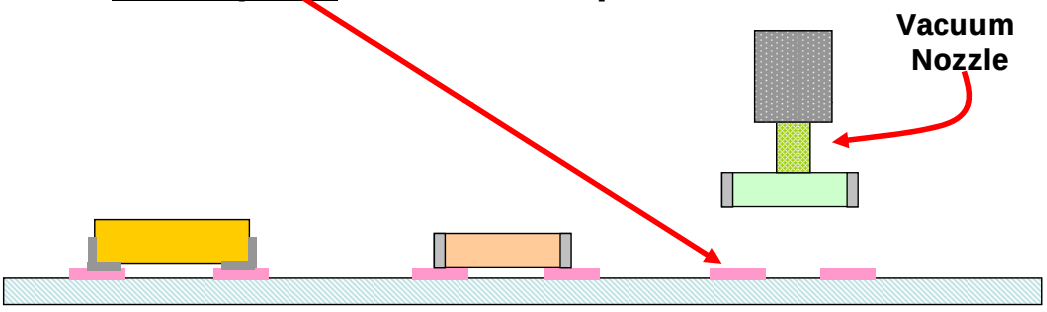


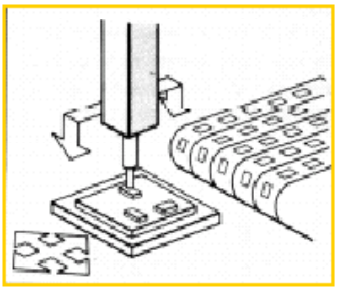
- Pin Transfer
- Pressure Syringe
- Screen Transfer

Method	Advantages
Pin transfer	Compact system simple, little maintenance, simultaneous dot placement, accepts pre-loaded mixed print boards, controls adhesive quantity
Screen Transfer	Simultaneous dot placement, simple process, uniform dot height
Pressure Syringe	Handles irregular surfaces, accepts mixed-print boards, control adhesive quantity, closed system not subject to outside influences, accepts most adhesives

SMD Assembly- Placing Components

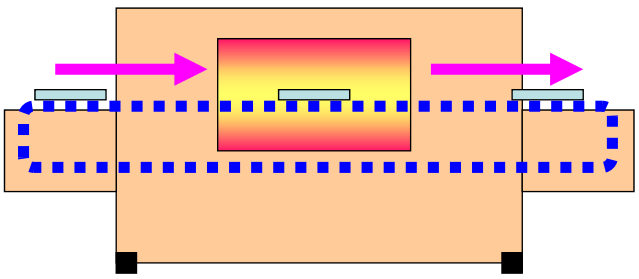
SMT parts are placed (by automatic pick and place equipment) onto solder paste covered land patterns.



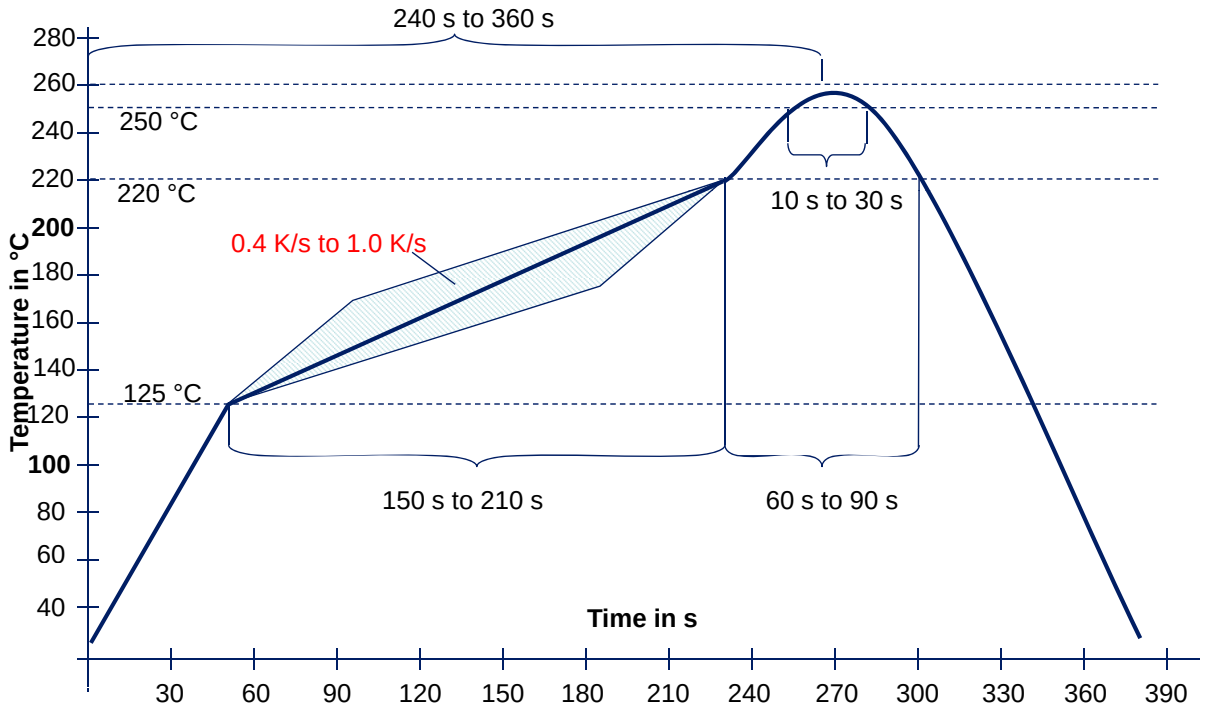


SMD Assembly- Reflow Soldering

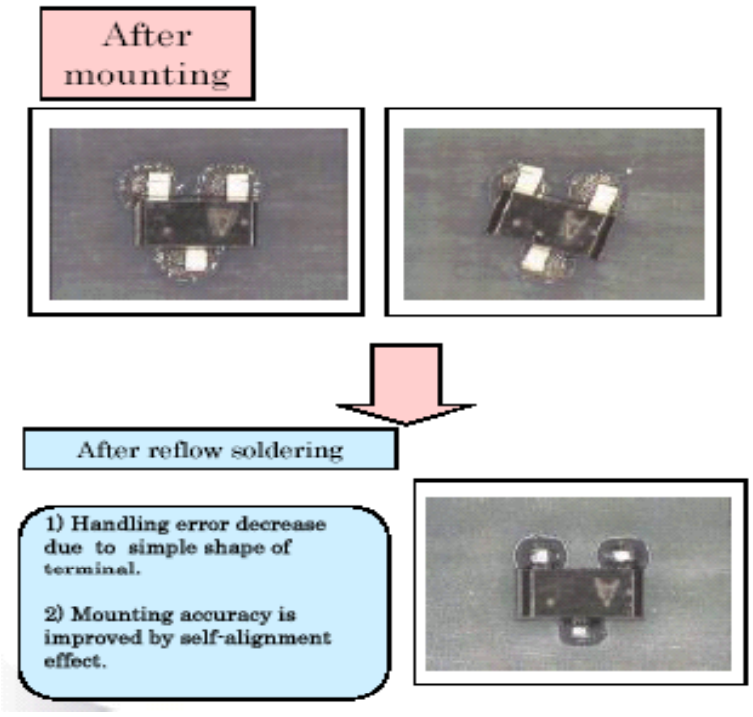
Circuit board is run through a reflow soldering oven. Where the solder paste liquefies, and electrically connects the SMT component terminations to the circuit board land patterns. As the circuit board moves out of heating zone the liquid solder solidifies mechanically fixing the SMT components to the circuit board.



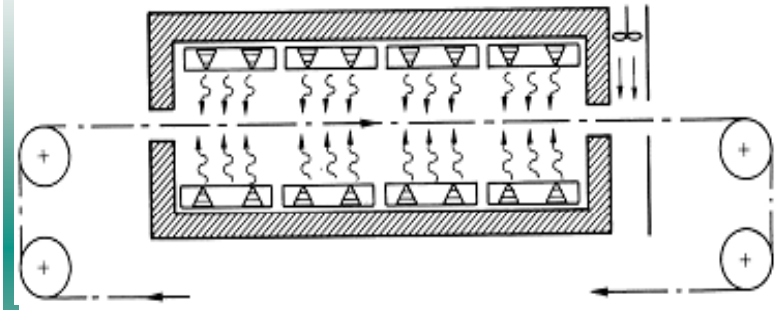
Soldering Temperature Profile: Reflow

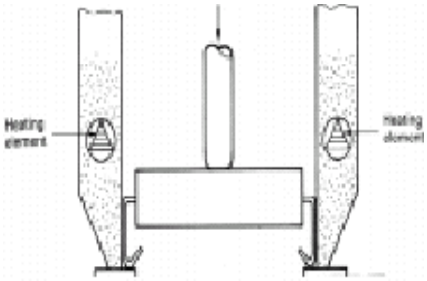


Advantage: Reflow Soldering

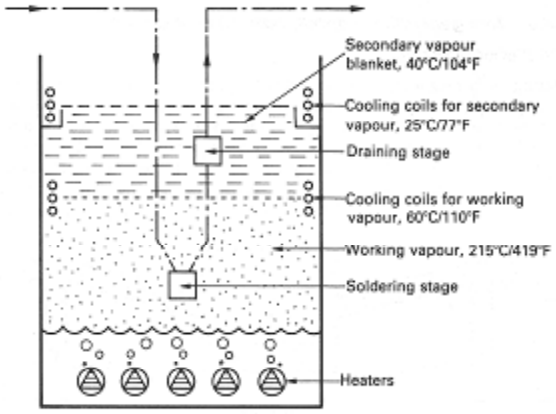


Heating Methods-Reflow Soldering





- IR Heating
- Resistance Soldering
- Vapor Phase heating
- Hot air Heating
- Laser heating



Summery: Assembly

- Usually Assembly and Manufacturing of PCB take place at two different places.
- These processes are not that simple as they appear on the slides.
- Green (lead and toxic free) products are being promoted, Which makes the process costly and more complicated.
- The exact and correct recipes is not fixed, has to be tuned with particular machine and raw material supplier.
- Quality of raw material should be strictly controlled.

Wakeup Please lets have Some Food….