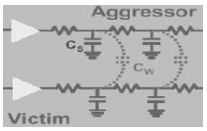

Crosstalk & Parallelism

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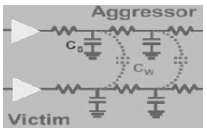
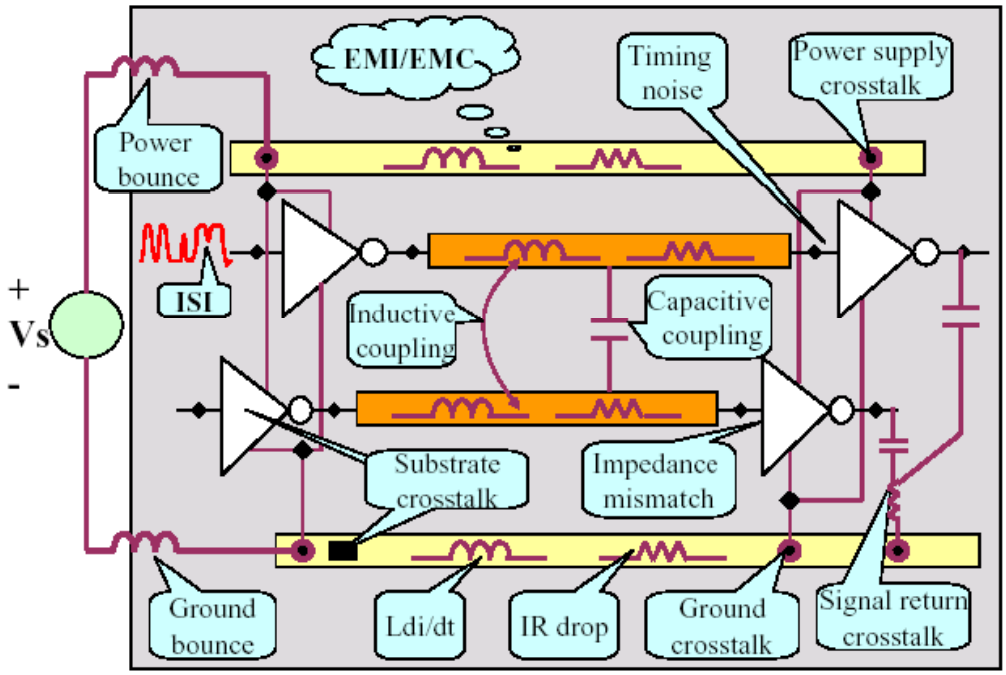
FAST-NU, Islamabad



Today's Topics

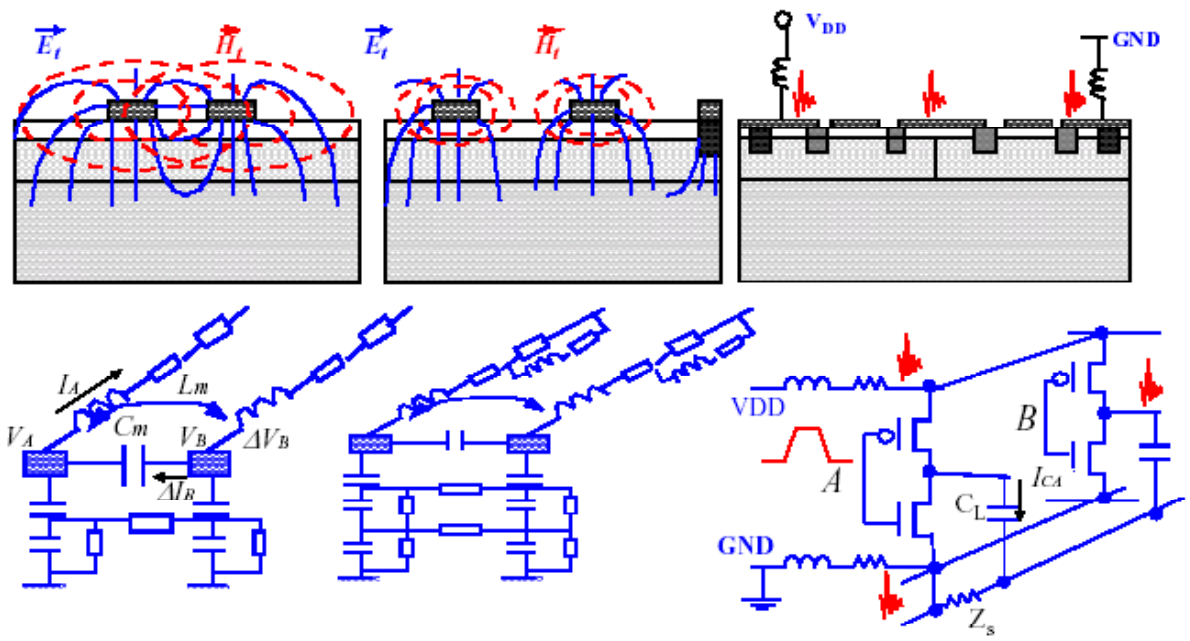
- Crosstalk and Parallelism
  - Overview
  - Definition, Sources and Dependence
  - Crosstalk Models for simulation
  - Near End and Far End Crosstalk
  - Crosstalk dependence on termination
  - Impedance variation due to crosstalk
  - Case Study

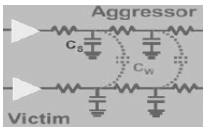
Noise: Cumulative Overview



Noise Coupling Via Interconnect

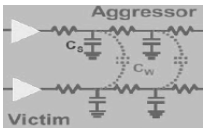
❑ Near Field Coupling ❑ Substrate Coupling ❑ Power/Ground Crosstalk ❑ Signal Return Crosstalk



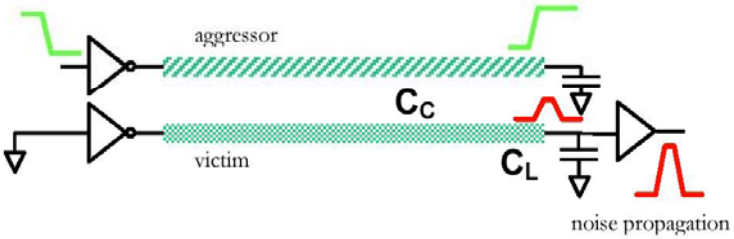


Crosstalk

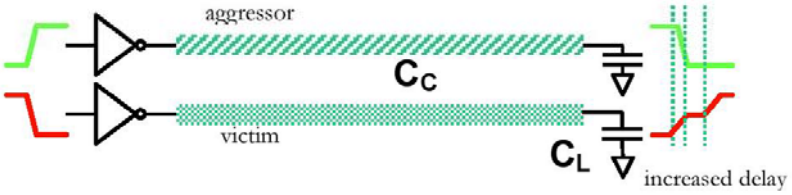
- Mutual interference between two circuits give rise to the crosstalk.
- Inductive Crosstalk (proportional to di/dt of the driven line).
- Capacitive Crosstalk (proportional to dv/dt of the driven line).
- Common Path Crosstalk - Resistive Crosstalk proportional to the current flow.
- Inductive crosstalk ≥ capacitive crosstalk in digital circuits.



Crosstalk

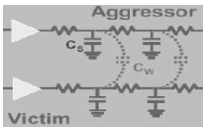


- Crosstalk occurs at
  - On-Chip
  - On Chip Package
  - On PCB
  - On Connectors
  - On Connector Cables

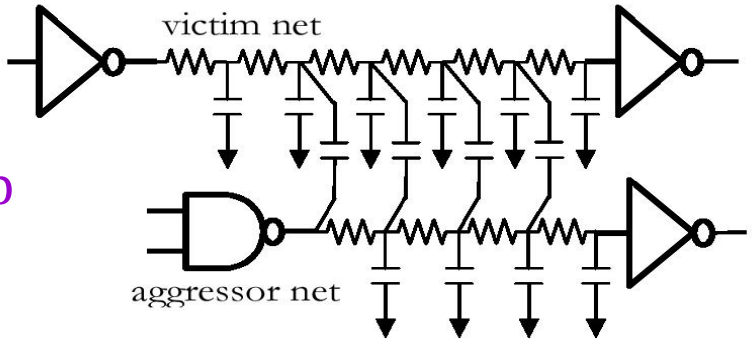


- Crosstalk change and modify the Zo and propagation delay. This effects system level timing hence Signal Integrity.
- Crosstalk depends upon data pattern, line to line spacing and switching rates.

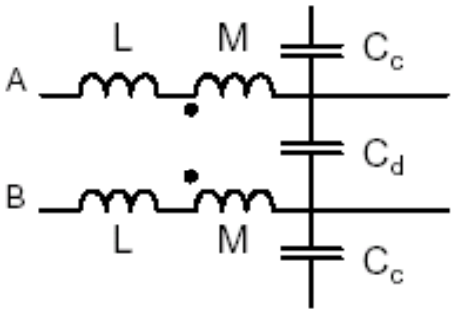
Crosstalk Circuit Model



On-Chip



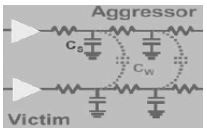
Off-Chip

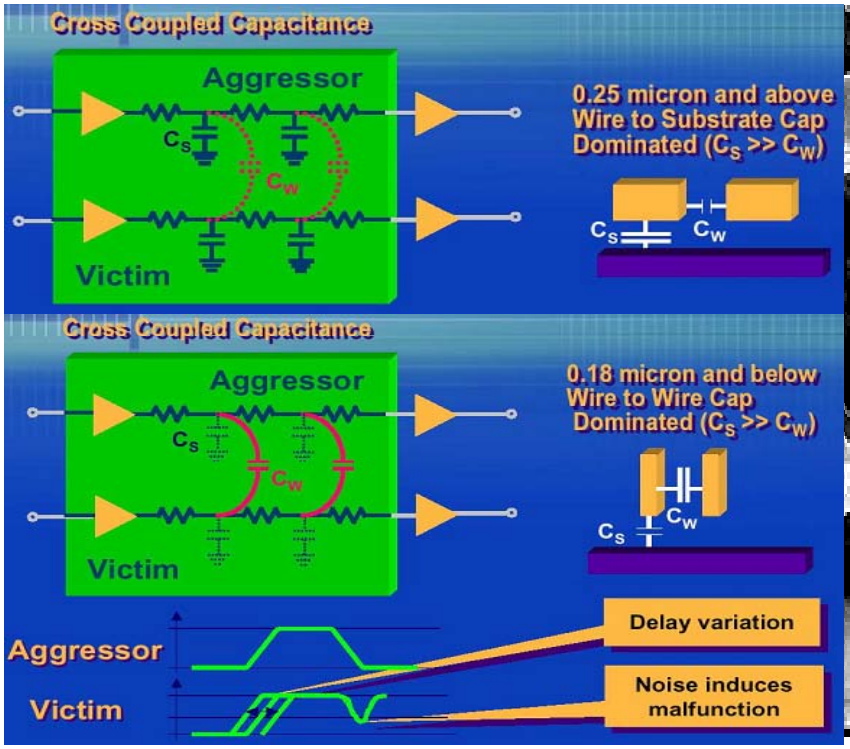


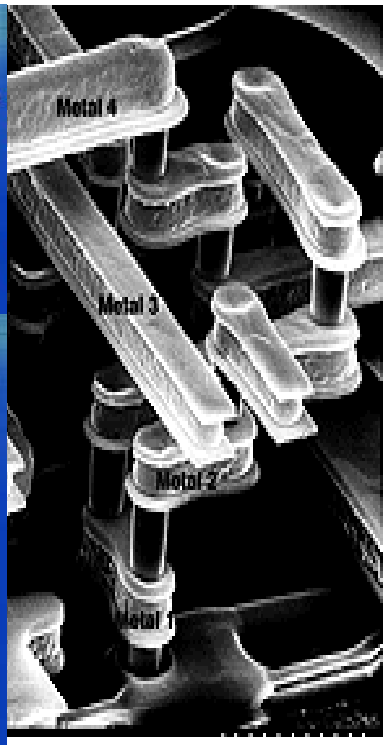
$$V_{noise,L_m} = L_m \frac{dI_{driver}}{dt}$$

$$I_{noise,C_m} = C_d \frac{dV_{driver}}{dt}$$

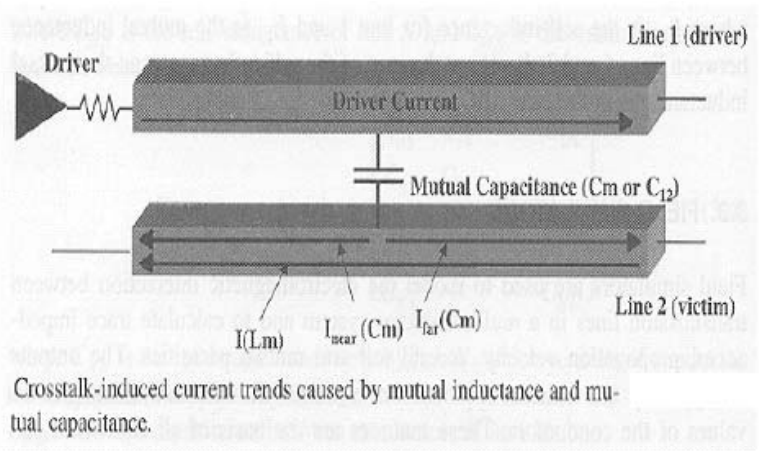
Inside IC: Cap Dominates







Crosstalk: Mutual Capacitance & Inductance

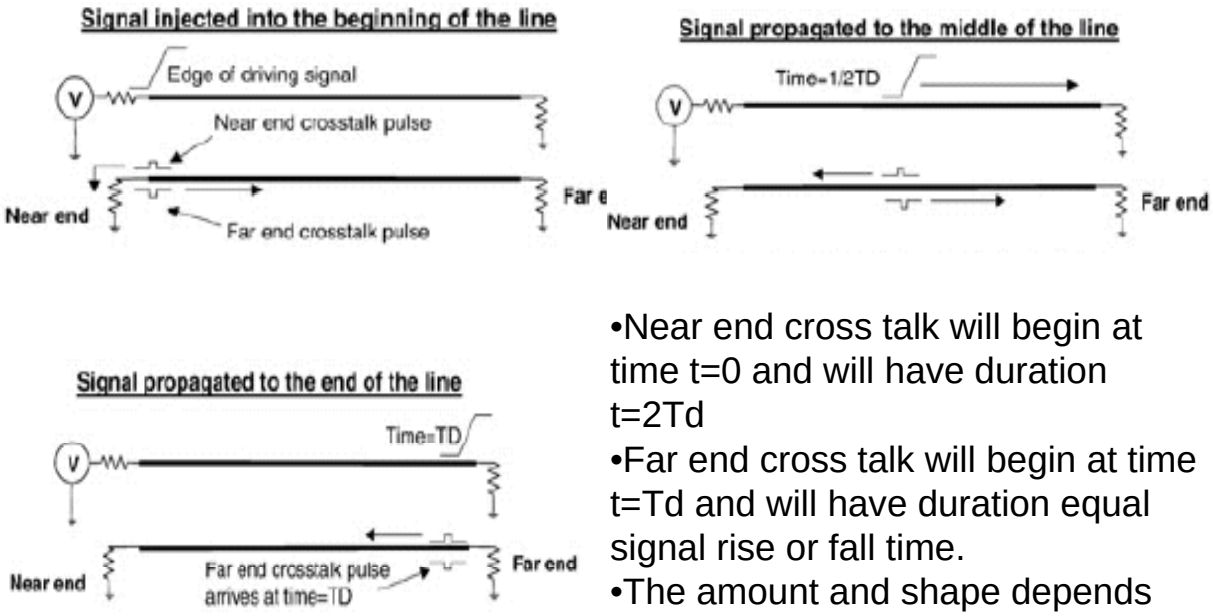


Crosstalk-induced current trends caused by mutual inductance and mutual capacitance.

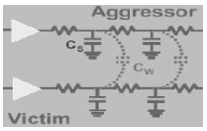
- Current induced by capacitive coupling goes to both directions
- Current induced by inductive coupling goes opposite to the drive current

$$I_{near\text{-}end} = I(L_m) + I_{near}(C_m)$$
$$I_{far\text{-}end} = I_{far}(C_m) - I(L_m)$$

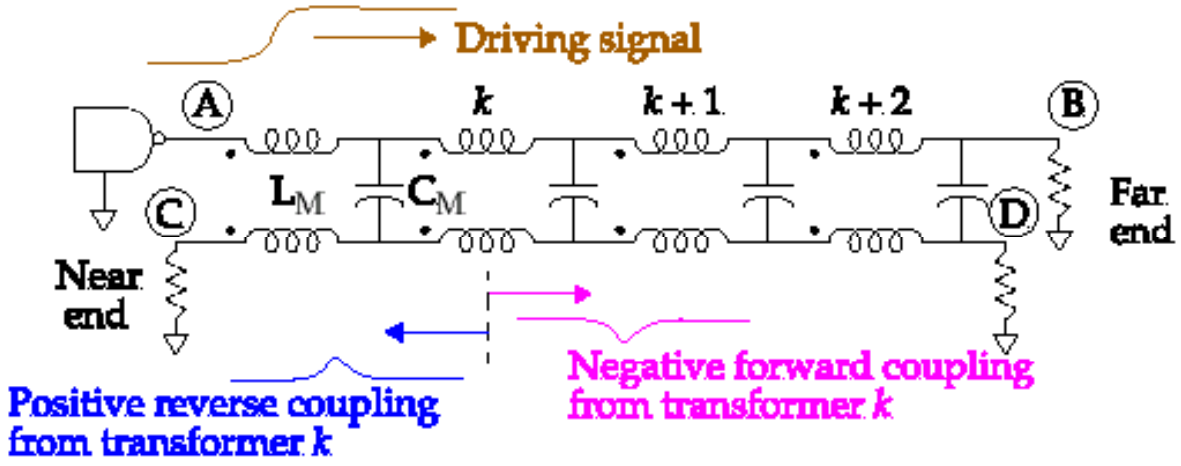
Near end and Far end Crosstalk

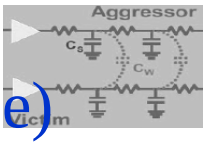


- Near end cross talk will begin at time t=0 and will have duration t=2Td
- Far end cross talk will begin at time t=Td and will have duration equal signal rise or fall time.
- The amount and shape depends upon the coupling and termination

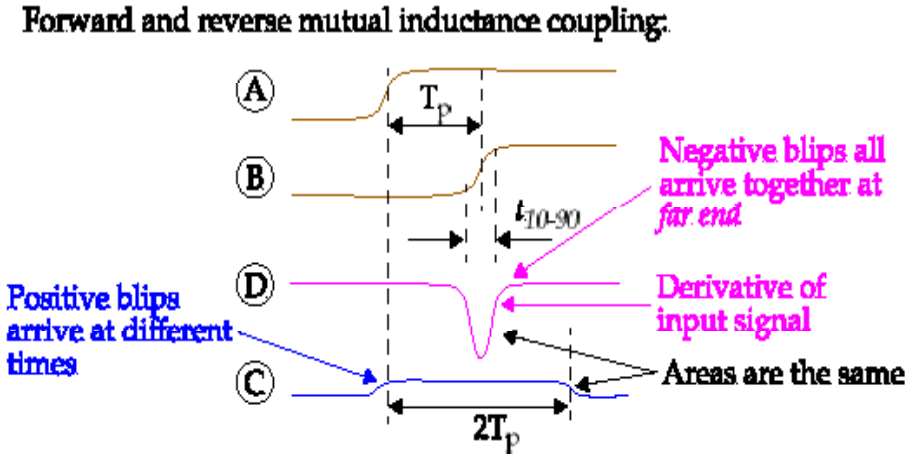


Near-end and far-end crosstalk

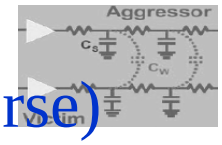




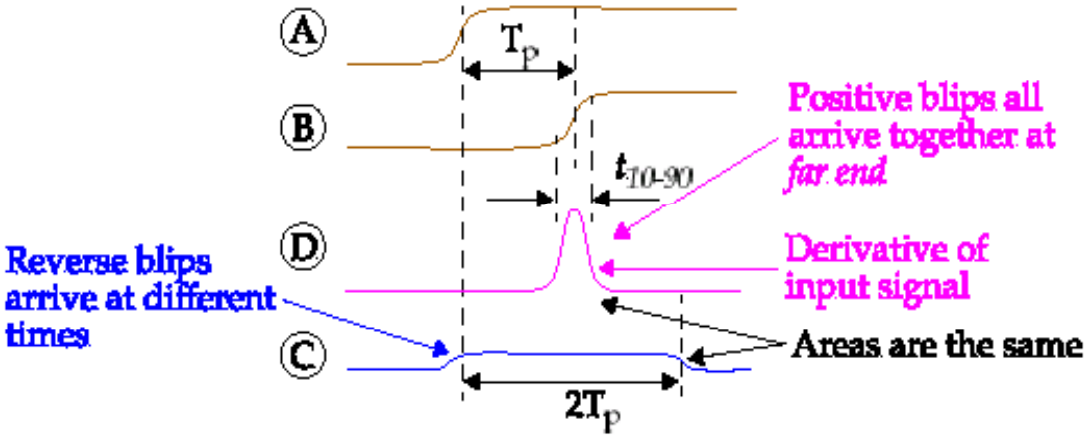
Inductive Coupling (Forward & Reverse)



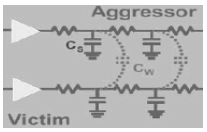
- The negative blip size at the far end is proportional to the total mutual inductance.
- Lengthening the line increases the size of blip at D.
- Height of the positive reverse coupling peak length of line.



Capacitive Coupling (Forward & Reverse)



- The two forward effects cancel at D.
- Striplines are well balanced between inductive and capacitive coupling.
- Microstrip electric field lines travel through air (cap coupling smaller)yielding small negative forward coupling coefficient.



Total Crosstalk

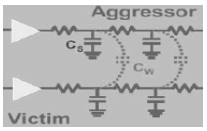
Combining Mutual Inductive and Capacitive Coupling:

- Amplitude of the crosstalk waves may be approximated by

$$V_f = \frac{1}{2}\left\{\frac{L_M}{L} - \frac{C_M}{C}\right\}\frac{T_P}{T_r}V_d$$

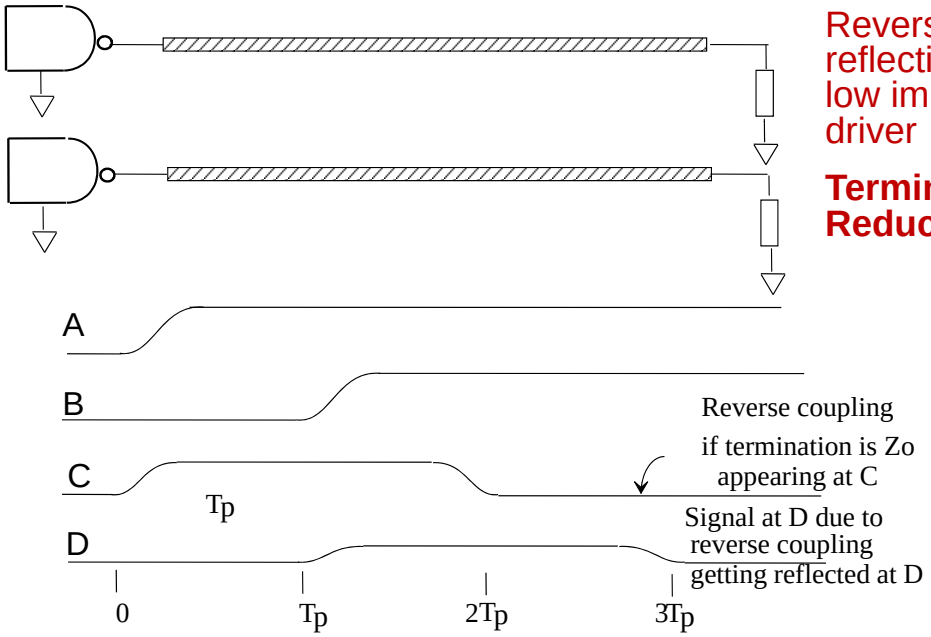
$$V_b = \frac{1}{4}\left\{\frac{L_M}{L} + \frac{C_M}{C}\right\}V_d \ (\text{for} T_r < 2T_P)$$

- Forward crosstalk could be made zero by a proper line arrangement



Total Crosstalk

How Near-End Crosstalk becomes a Far-End Problem

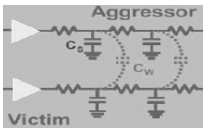


Reverse coupling reflecting from a low impedance driver

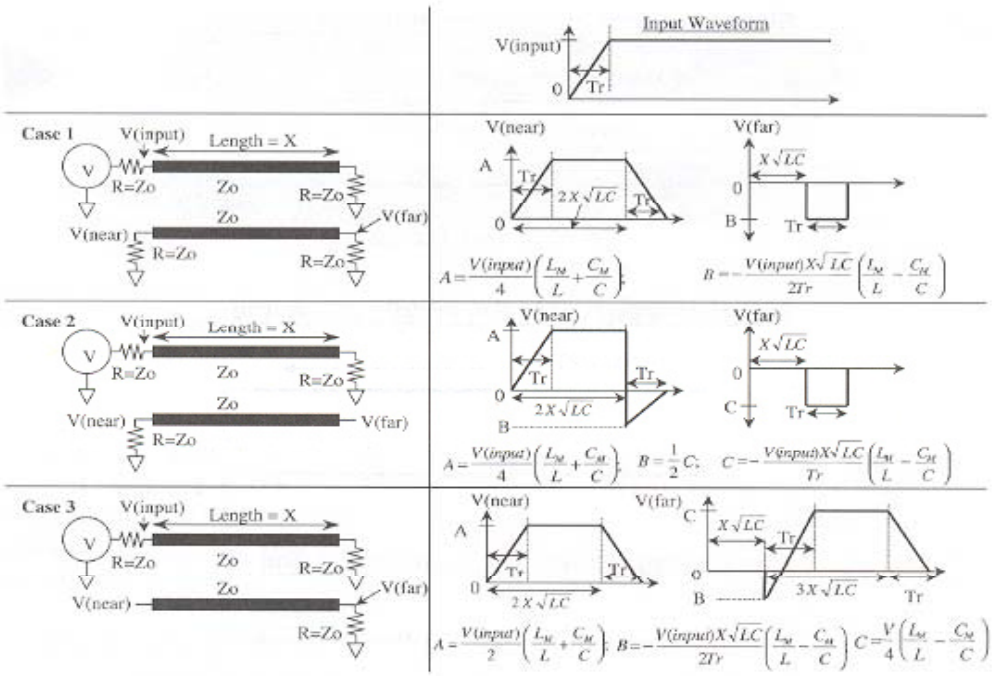
Termination to Reduce Crosstalk

Reverse coupling if termination is Zo appearing at C

Signal at D due to reverse coupling getting reflected at D

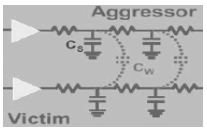


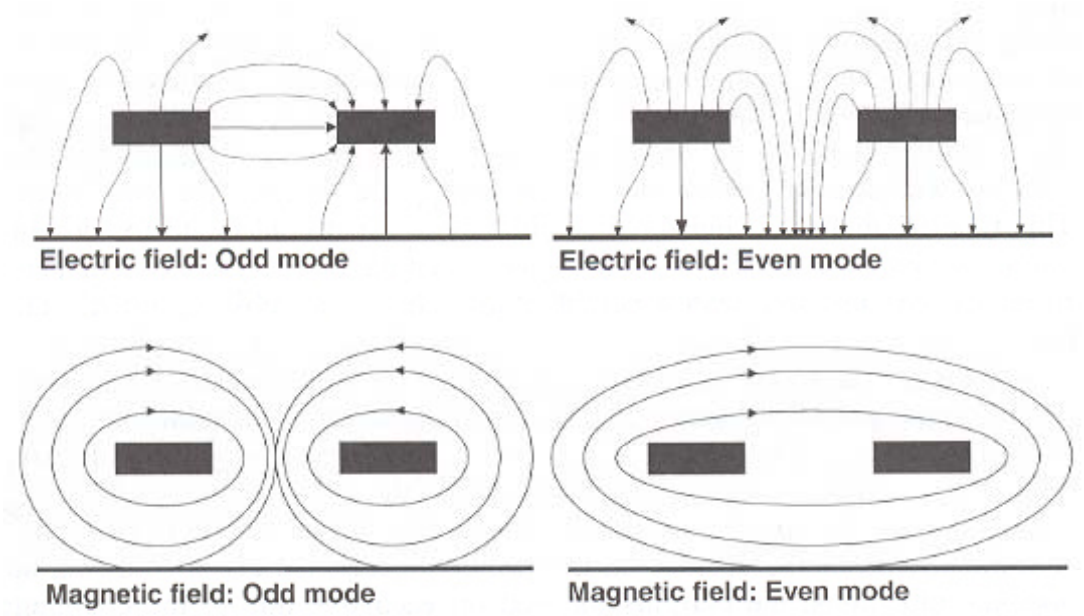
Near, Far end Crosstalk & Termination



Digital crosstalk noise as a function of victim termination.

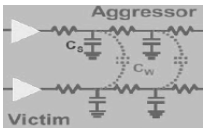
Odd and Even Mode Fields

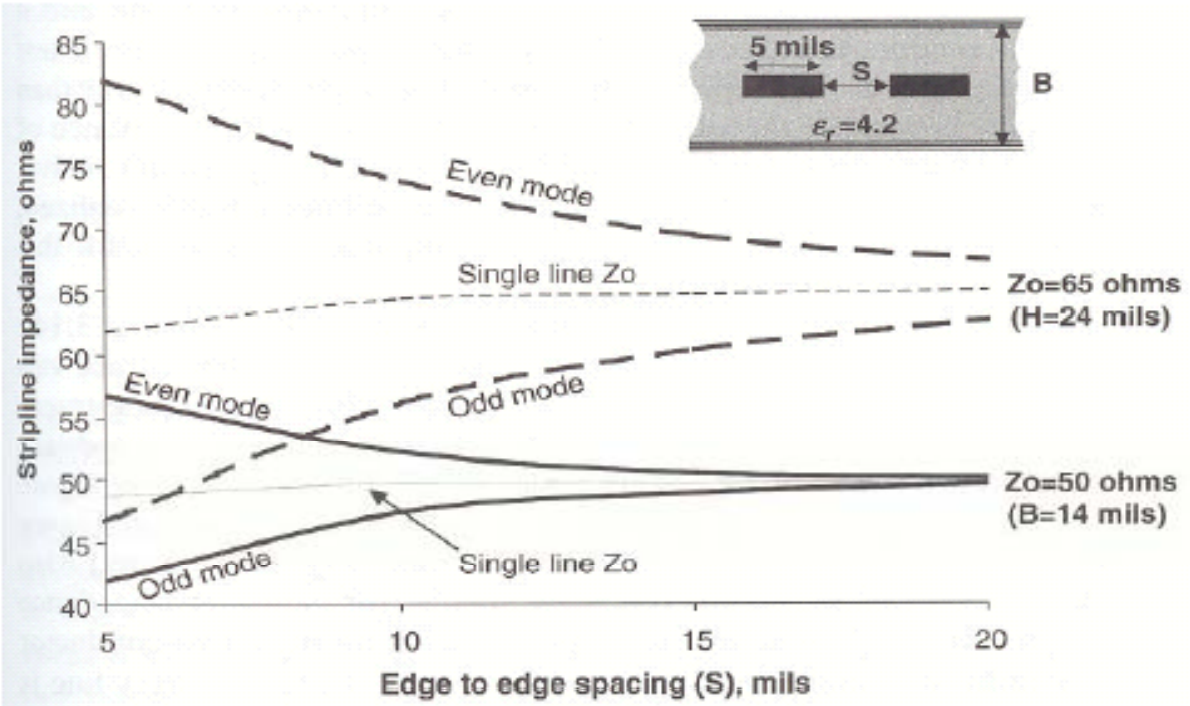


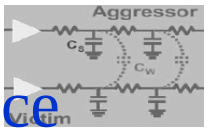


Odd- and even-mode electric and magnetic field patterns for a simple two-conductor system.

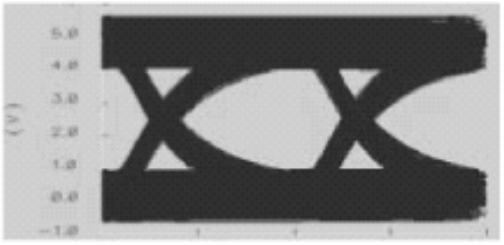
Impedance variation and Crosstalk



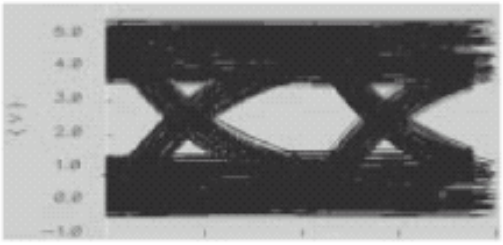




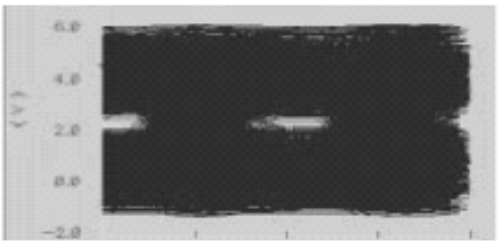
Crosstalk: Switching Pattern Dependence



a: Aggressors Switching in Same Direction



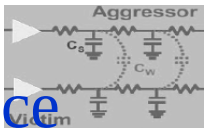
b: Adjacent Interconnect Grounded



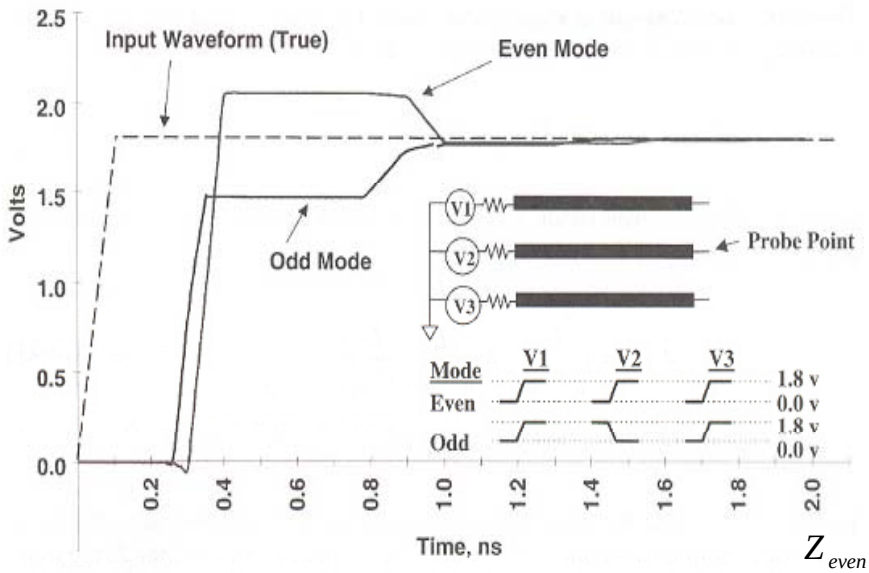
c: Aggressors Switching in Random Fashion

These are simulated eye diagrams for parasitics extracted for a 0.05 micron technology with an inter-layer dielectric thickness of 0.21microns

Fig. 3: Eye Diagrams for 700 MHz Signaling Over 1.5 mm Metal 1 Interconnect for parasitics extracted for a 0.05 micron technology with minimum spaced wire geometry.



Crosstalk: Switching Pattern Dependence



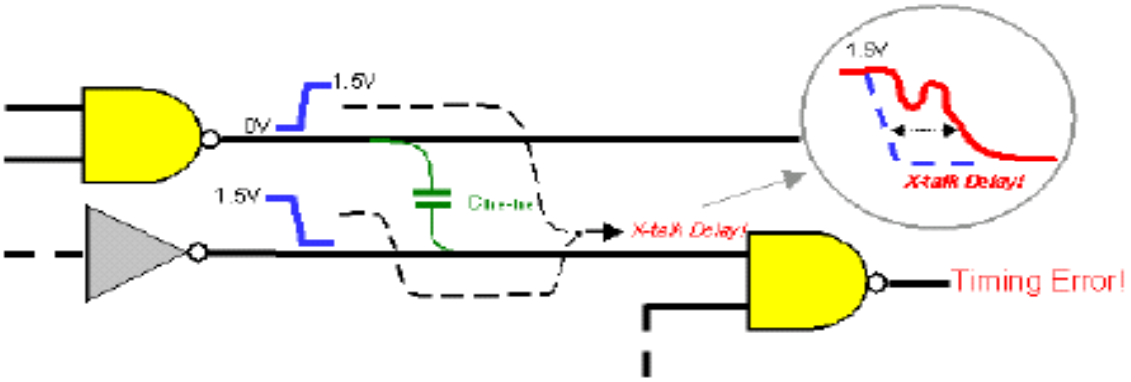
Effect of switching patterns on a three-conductor system.

$$C_{even} = C_{11} - C_{12}$$
$$L_{even} = L_{11} + L_{12}$$
$$C_{odd} = C_{11} + C_{12}$$
$$L_{odd} = L_{11} - L_{12}$$

$$Z_{even} = \sqrt{\frac{L_{even}}{C_{even}}} = \sqrt{\frac{L_{11} + L_{12}}{C_{11} - C_{12}}}$$

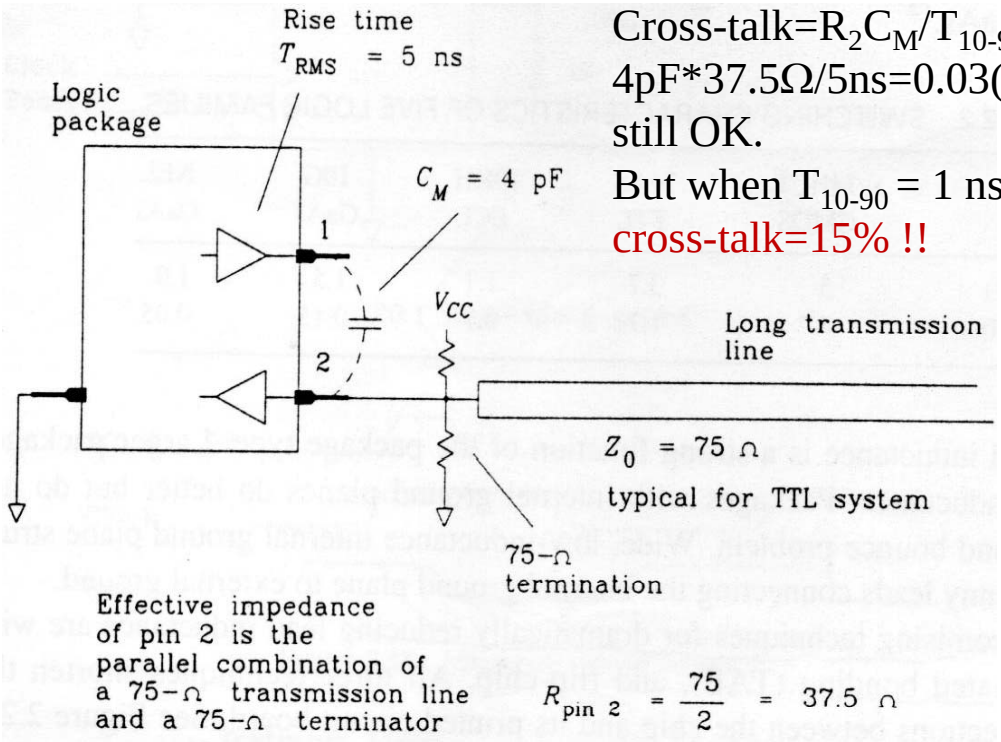
$$Z_{odd} = \sqrt{\frac{L_{odd}}{C_{odd}}} = \sqrt{\frac{L_{11} - L_{12}}{C_{11} + C_{12}}}$$

Noise-on-Delay Effect: Crosstalk



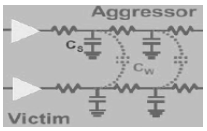
$$\Delta t = V_{noise} \frac{t_{r,f}}{V_{sw}}$$

Example



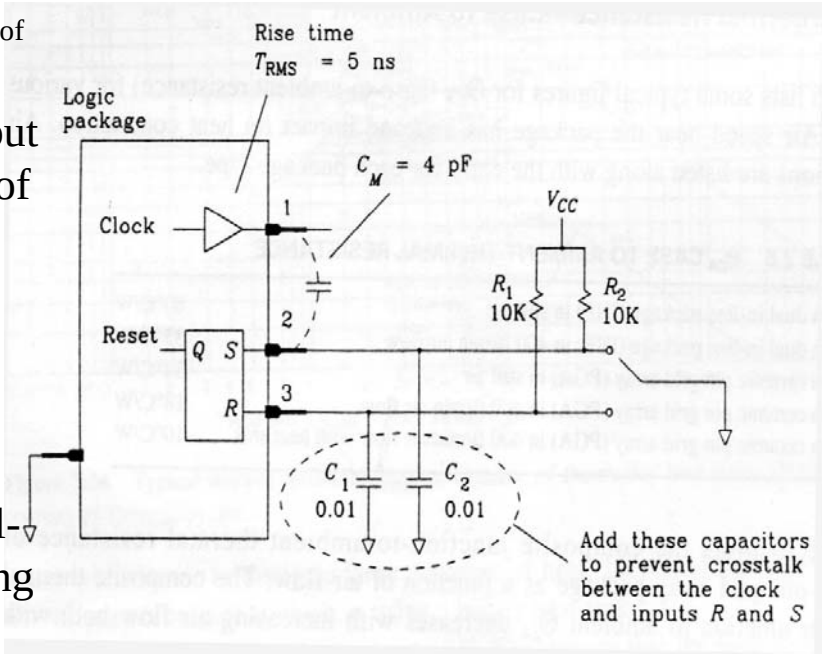
Cross-talk=$R_2C_M/T_{10\text{-}90,}$ = 4pF*37.5Ω/5ns=0.03(3%) still OK.

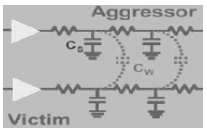
But when $T_{10\text{-}90}$ = 1 ns, cross-talk=15% !!



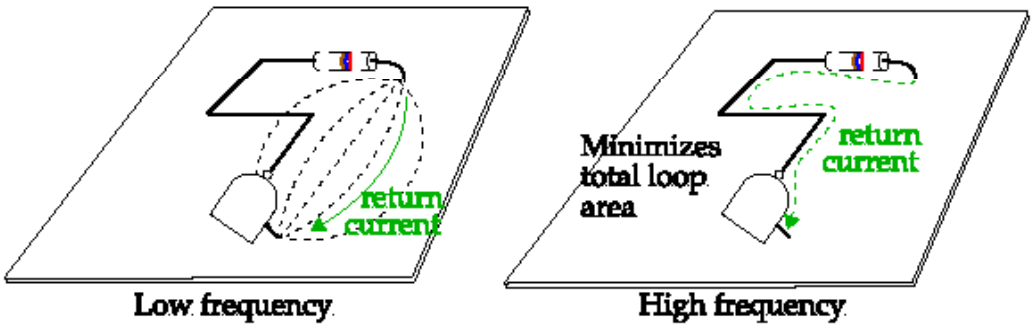
Example

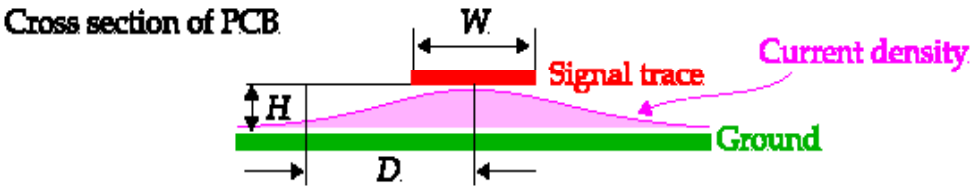
- Cross-talk=$C_M R_{(\text{input R of receiver})} / T_r$
- It is still OK, if the input has a parallel small R of 75Ω. Cross-talk=3%.
- If R2 = 10K (ie Open Collector), crosstalk=800%.
- Rule: Add capacitors connected to large pull-up resistors for reducing cross-talk.





Crosstalk vs. Geometry of Traces

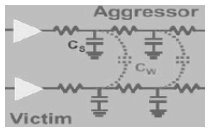




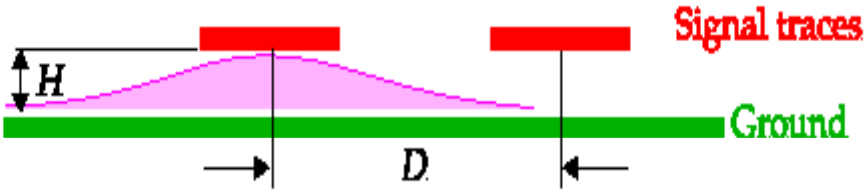
Current density for a point D inches away from trace.

$$i(D) = \frac{I_0}{\pi H} \frac{1}{1 + (D/H)^2} A/\text{in.}$$

Crosstalk vs. Geometry of Traces



The induced voltages are proportional to the *derivative* of the driving signal, e.g., faster rise times produce a more significant effect.

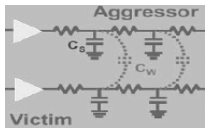


Ratio of measured noise voltage and driving step size

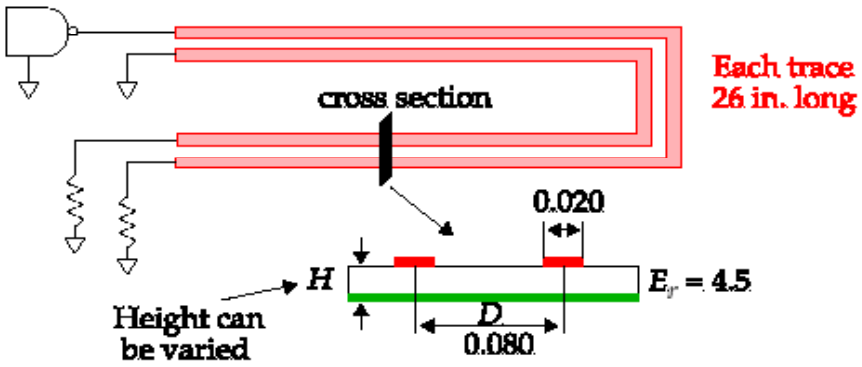
$$\text{Crosstalk} = \frac{K}{1+(D/H)^2}$$

where K depends on the rise time and length of interfering traces (<1).

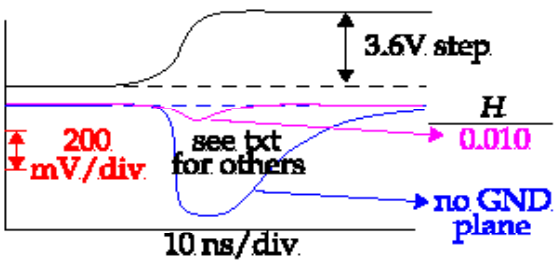
Crosstalk in Solid GND Plane

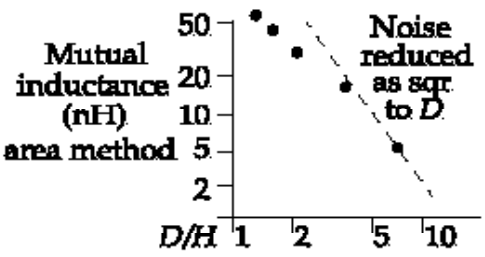


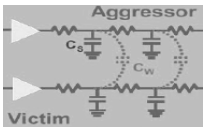
Experiment to test the D/H dependency in this equation.



Here, the height H can be changed by adding dielectric plates.

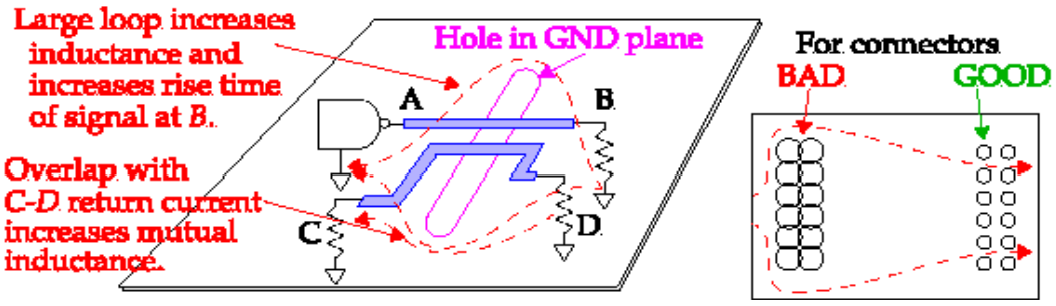






Crosstalk in Slotted GND Plane

Slotted GND planes are a big mistake:



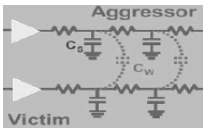
You may be tempted to do this when you run out of room on the regular routing layers and *cram* a trace in on the GND plane.

The effective inductance in series with *A-B* is approximated by:

$$L = 5D\ln\left(\frac{D}{W}\right)$$

D = perpendicular extent of current diversion away from signal trace, in.
W = trace width, in.

Inductance is almost completely independent of slot *width*.



Crosstalk in Slotted GND Plane

The worse case is a long line with the apparent src resistance on either side of the inductance is Z_0.

The results 10-90% rise time of the *L/R* filter (weighted in with the natural signal rise time) is:

$$T_{10\text{-}90\ L/R} = 2.2\frac{L}{2Z_0} \longrightarrow T_{composite} = \sqrt{(T_{10\text{-}90\ L/R})^2 + (T_{10\text{-}90\ signal})^2}$$

For a short line driving a heavy capacitive load C, the 10-90% rise time (assuming critical damping) is: $T_{10-90} = 3.4\sqrt{LC}$

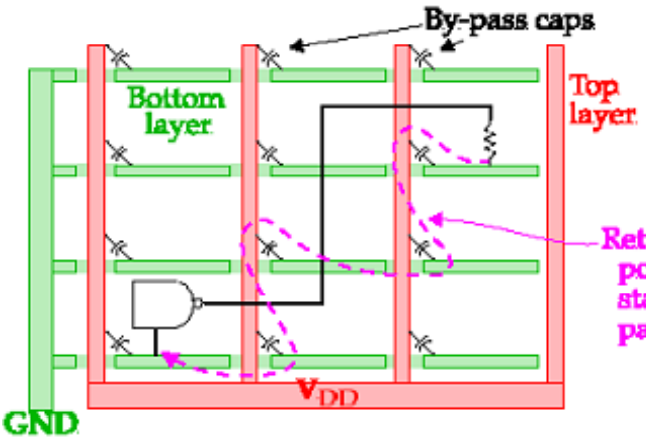
The cross coupling voltage is derived by the mutual inductance and the time rate of change in current in the driver. $V_{crosstalk} = \frac{\Delta I}{T_{10\text{-}90}} L_M$

For a long line, the ΔI is the drive voltage/*characteristic impedance*.

$$V_{crosstalk} = \frac{\Delta V}{T_{10\text{-}90} Z_0} L_M$$

Crosstalk in Crosshatched GND Plane

If you are forced to use a two layer board:



First estimate the self-inductance:

$$L \approx 5\,Y \ln\left(\frac{X}{W}\right)$$

X = hatch width, in.
W = trace width, in.
Y = trace length, in.

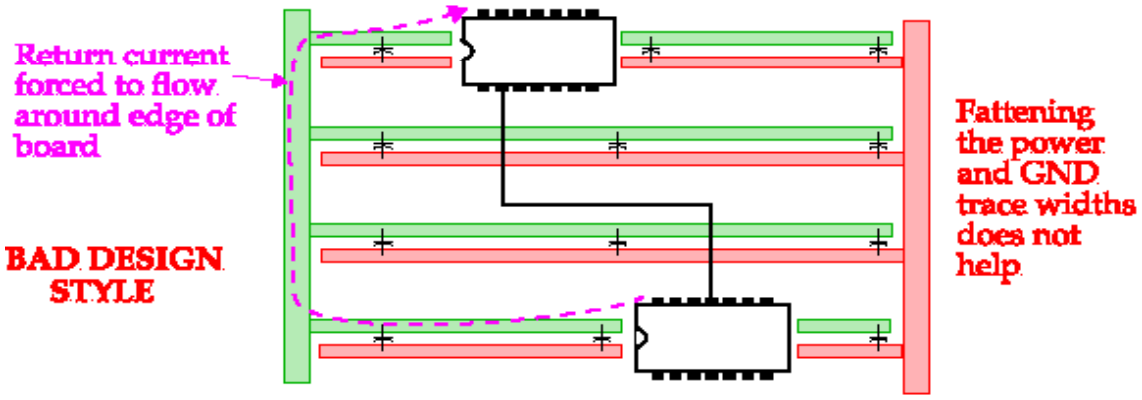
$$V_{\text{crosstalk}} = \frac{\Delta V}{T_{10\text{-}90} Z_0} L_M$$

Note that signals are interleaved with the power and GND routing.
This layout increases *mutual inductance*.
Appropriate for low-speed CMOS and TTL design – not high-speed logic.
Current returns equally well through the GND and power wires.

If two traces are separated by a larger distance D,

$$L_M = \frac{5\,Y \ln(X/W)}{1 + (D/X)^2}$$

Crosstalk with PWR and GND Fingers



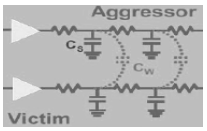
Both power and GND are routed on the same layer.

The diversion of the current introduces a huge amount of *self* and *mutual inductance*, both modeled as.

$$L \approx 5\,Y \ln\left(\frac{X}{W}\right)$$

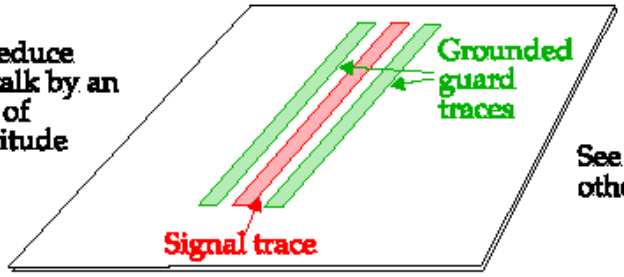
X = board width!
W = trace width
Y = trace length

Guard Rings: Reduce the Crosstalk



These are used a lot in analog design:

Can reduce crosstalk by an order of magnitude



See text for other illustrations

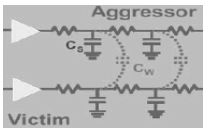
However, for digital, *solid GND planes* provide most of the benefits of guard traces (guard traces add very little).

As a rule of thumb, coupling between microstrip signal lines is *cut in half* by inserting a third line (GNDed at both ends) between them.

Coupling is halved yet again if the third line is *frequently* tied (through vias) to the GND plane.

In digital with a solid GND plane, the reduction in crosstalk is not significant even if it's possible to insert a *guard* trace between two traces.

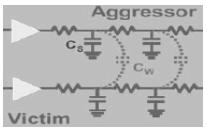
How much Crosstalk?

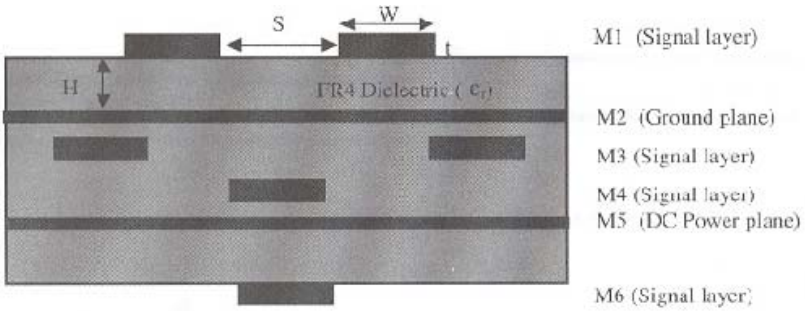


How much crosstalk is too much?

- Crosstalk level of 1-3% between adjacent wires is fine
- Assumes that there exists solid ground plane
- Each wire interacts only with its nearest neighbours
- Cross-coupling from other more remote wires is negligible

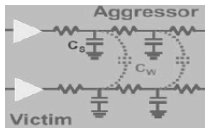
Rule to Minimize Crosstalk

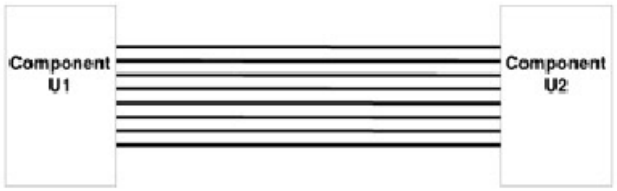


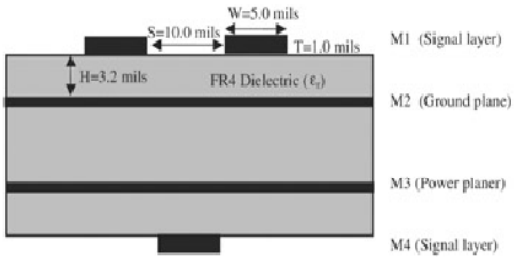


- Widen spacing S between the lines as much as routing restrictions will allow
- Minimize H while achieving the target impedance of the design
- Use differential routing techniques for critical nets, such as system clock if allowed
- Routing adjacent metal layers orthogonal if there is significant inter-layer coupling
- If possible, routing the signals on a strip layer or as an embedded microstrip to eliminate velocity variation.
- Minimize parallel run lengths between signals, routing with short parallel sections and minimize long coupled sections between nets.
- If possible, use slow edge rates (with extreme caution on timing uncertainty)

Case Study: False Triggering





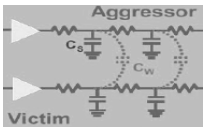


Problem:

8 Bit wide Bus, Four Layer board
Driving Buffer Rs = 30 Ω
Swing = 2V, Length of trace= 5 in
Center-Center Spacing =15 Mil,
Zo(with Out Cross talk) = 50 Ω
ε_r= 4.0 (FR4)
Input Buffer capacitance << ignored
Mutual inductance = 0.54 nH/in
Mutual Capacitance = 0.079 pF/in

Goals is to Determine:

1. Self inductance and Capacitance.
2. Max impedance variation due to Crosstalk?
3. Max velocity variation due to Crosstalk?
4. Input buffer at U2 will switch at 1.0V, if there is possibility of false triggering?



Case Study: False Triggering

1. Self Inductance and Capacitance:

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[1 + \frac{12H}{W}\right]^{\frac{-1}{2}} + F - 0.217(\varepsilon_r - 1)\frac{T}{\sqrt{WH}}$$

$$\varepsilon_r(FR4) = 4 \ , W/H = 5/3.2 \Rightarrow F = 0$$

$$\varepsilon_e = \frac{4+1}{2} + \frac{4-1}{2}\left[1 + \frac{12(3.2)}{5}\right]^{\frac{-1}{2}} + 0 - 0.217(4-1)\frac{1.0}{\sqrt{5.0(3.2)}}$$

$$\varepsilon_e = 2.84$$

$$v = \frac{c}{\sqrt{\varepsilon_r}} = \frac{3.0\times10^8 m/s}{\sqrt{2.84}} = 1.78\times10^8 m/s$$

$$TD = \frac{length\sqrt{\varepsilon_r}}{c} = \frac{5.0in}{1.78\times10^8 m/s}\left(\frac{0.0254m}{1.0in}\right) = 713ps$$

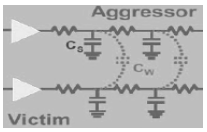
$$Velocity(in/ps) = \frac{5in}{713ps} = 0.0070\ in/ps$$

$$TD(per\ inch) = \sqrt{LC} = \frac{713ps}{5.0in} = 142.6\,ps/in$$

$$\because Z_o = \sqrt{\frac{L}{C}} = 50\Omega$$

$$\Rightarrow C = \frac{TD}{Z_o} = \frac{\sqrt{LC}}{\sqrt{L/C}} = \frac{142.6ps}{50} = 2.85pF$$

$$\Rightarrow L = TD \times Z_o = \sqrt{LC} \times \sqrt{L/C} = 7.13nH$$



Case Study: False Triggering

2. Max Velocity variation due to Crosstalk

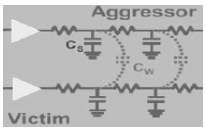
First, let's evaluate the effects of common-mode propagation (all bits switching in phase). Assume that line 2 represents a conductor in the middle of the 8-bit bus.

Ground plane

Common-mode switching pattern.

- Even-mode capacitance of conductors 2 and 1 = C_{22} - C_{12}
- Even-mode capacitance of conductors 2 and 3 = C_{22} - C_{23}
- Equivalent capacitance of conductor 2 = C_{22} - C_{12} - C_{23}
- Even-mode inductance of conductors 2 and 1 = L_{22} + L_{12}
- Even-mode inductance of conductors 2 and 3 = L_{22} + L_{23}
- Equivalent inductance of conductor 2 = L_{22} + L_{12} + L_{23}

Case Study: False Triggering



$$Z_{2,common} = \sqrt{\frac{L_{22} + L_{12} + L_{23}}{C_{22} - C_{12} - C_{23}}}$$

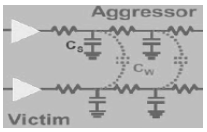
$$Z_{2,common} = \sqrt{\frac{7.13nH + 0.54nH + 0.54nH}{2.85\,pF - 0.079\,pF - 0.079\,pF}} = 55.26\ \Omega$$

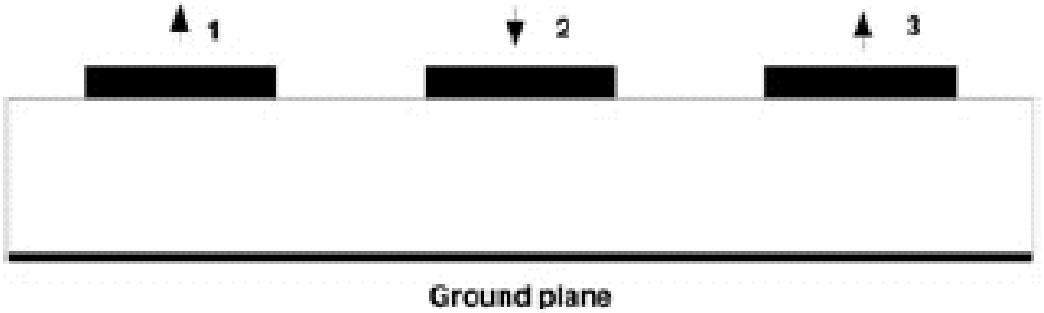
$$TD_{2,common} = \sqrt{(L_{22} + L_{12} + L_{23})(C_{22} - C_{12} - C_{23})}$$

$$TD_{2,common} = \sqrt{(7.13nH + 0.54nH + 0.54nH)(2.85\,pF - 0.079\,pF - 0.079\,pF)}$$

$$TD_{2,common} = 148.6\,ps/in$$

Case Study: False Triggering

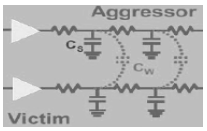




Differential switching pattern.

- Odd-mode capacitance of conductors 2 and 1 = $C_{22} + C_{12}$
- Odd-mode capacitance of conductors 2 and 3 = $C_{22} + C_{23}$
- Equivalent capacitance of conductor 2 = $C_{22} + C_{12} + C_{23}$
- Even-mode inductance of conductors 2 and 1 = $L_{22} - L_{12}$
- Even-mode inductance of conductors 2 and 3 = $L_{22} - L_{23}$
- Equivalent inductance of conductor 2 = $L_{22} - L_{12} - L_{23}$

Case Study: False Triggering



$$Z_{2,diffrential} = \sqrt{\frac{L_{22} - L_{12} - L_{23}}{C_{22} + C_{12} + C_{23}}}$$

$$Z_{2,diffrential} = \sqrt{\frac{7.13nH - 0.54nH - 0.54nH}{2.85\,pF + 0.079\,pF + 0.079\,pF}} = 44.8\,\Omega$$

$$TD_{2,diffrential} = \sqrt{(L_{22} - L_{12} - L_{23})(C_{22} + C_{12} + C_{23})}$$

$$TD_{2,diffrential} = \sqrt{(7.13nH - 0.54nH - 0.54nH)(2.85\,pF + 0.079\,pF + 0.079\,pF)}$$

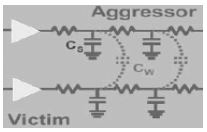
$$TD_{2,diffrential} = 135\,ps/in$$

Variation in velocity and impadance

$$44.8\Omega < Z_o < 55.26\Omega$$

$$135\,ps < TD < 148.6\,ps$$

Case Study: False Triggering

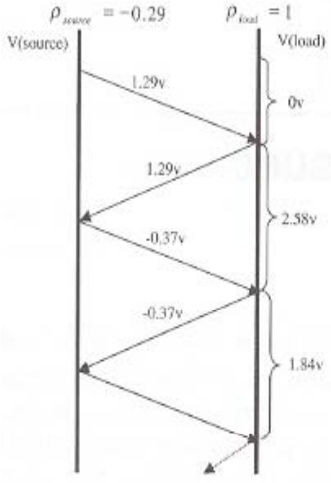


3. If Crosstalk will induce false triggering?

The signal will ring down to a minimum voltage of 1.84V.

Since the threshold voltage of this buffer was defined to be 1.0V, and signal does not ring back down to this value.

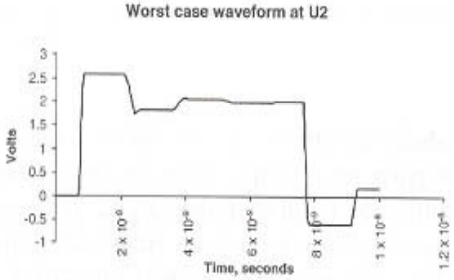
The signal integrity will not cause false triggering.



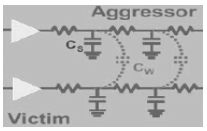
$$V_{initial} = Vs\frac{Zo}{Rs+Zo} = (2)\left(\frac{55}{30+55}\right) = 1.29$$

$$\rho_{source} = \frac{Rs-Zo}{Rs+Zo} = \frac{30-55}{30+55} = -0.29$$

$$\rho_{load} = \frac{Zl-Zo}{Zl+Zo} = \frac{\infty-55}{\infty+55} = 1$$

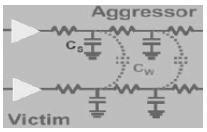


Calculation of the final waveform.



Summery

- There in no velocity variation due to Crosstalk in Striplines but there is in Microstrip.
- The nearest neighbor has greatest effect.
- Common mode (All bit in phase) and differential (only target out of phase) mode produce worst velocity and impedance variation.
- Low impedance line produces less impedance variation.
- The impedance of the trace is effected by the proximity of the neighbor traces even when they are not driven,
- Mutual parasitic falls off exponentially with trace-to-trace spacing.



Wakeup Please lets have Some Food....