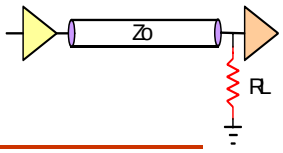
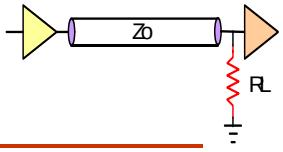


Impedance Control, Terminations, Differential Pairs and Buses

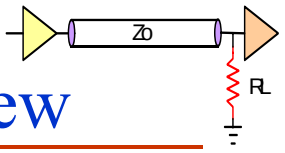
Rashad.M.Ramzan, Ph.D

FAST-NU, Islamabd

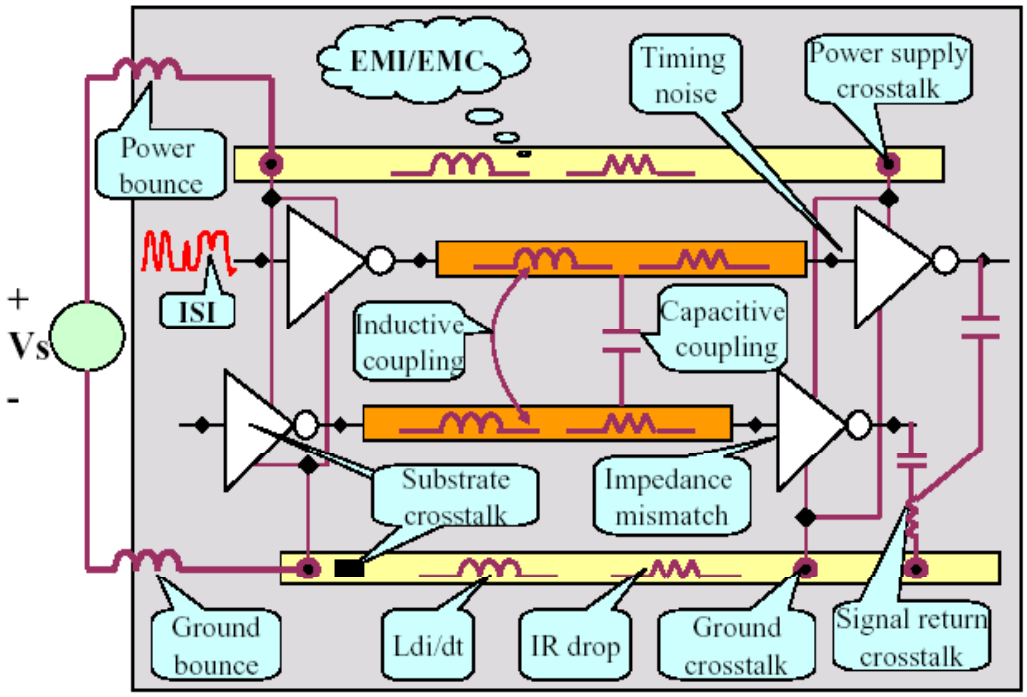


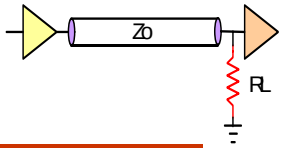
Today's Topics

- Impedance
  - Why Zo is important?
  - Basic Definition and Concept
  - Impedance Formula (Dependence on Geometry)
    - Stripline, Microstrip, Embedded Stripline, Embedded Microstrip
  - Even and Odd mode Impedance
- Termination
  - When termination is needed?
  - Types of Termination
    - End Termination, Split Termination, Series and Diode Termination
    - AC biasing
    - Termination of Coupled Differential Lines (Even and Odd Mode Impedance)
  - CASE STUDY (CLK and Bus Termination)



Noise: Cumulative Overview

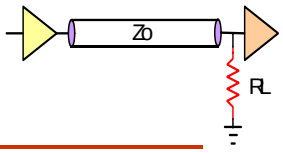


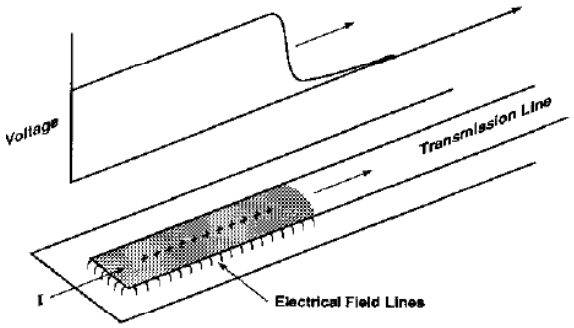


Why Z_o So Important?

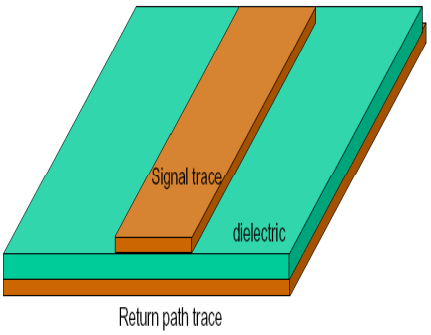
- If Zo do not change with the length of line life would have been much easier.
- Otherwise change in Zo is source of most of nasty problems in board and IC design.

Impedance Control

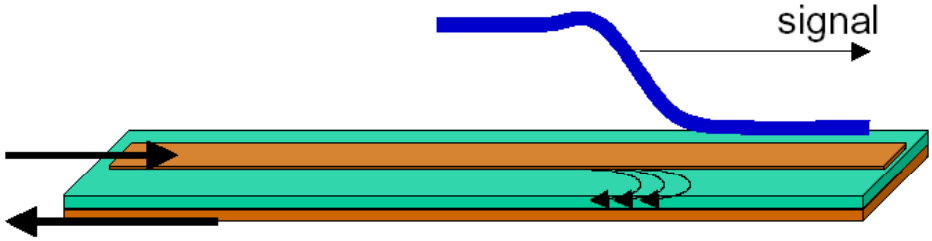




Signal moving down transmission line, frozen in time.

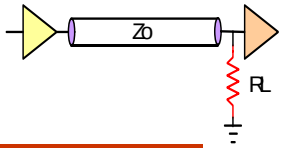


Character Impedance is instantaneous impedance the signal sees moving down the line.



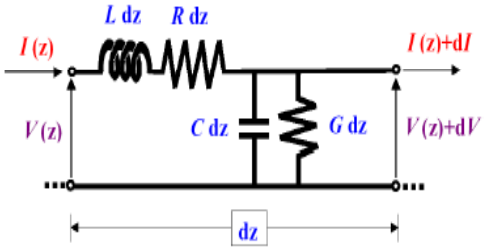
Current paths in a transmission line as the signal propagates. Note that the current returns to the source where ever the signal voltage is changing.

Derivation of Zo



$j\omega L(\Delta z) + R(\Delta z) = Z\Delta z$ (series impedance for length of line Δz)

$j\omega C(\Delta z) + G(\Delta z) = Y\Delta z$ (parallel admittance for length of line Δz)



Then

$$Z(\text{input}) = Z_o = \frac{(Z_o + Z\Delta z)(1/Y\Delta z)}{Z_o + Z\Delta z + 1/Y\Delta z}$$ (assuming the load is equal to the characteristic impedance)

$$Z_o\left(Z\Delta z + Z_o + \frac{1}{Y\Delta z}\right) = (Z_o + Z\Delta z)\frac{1}{Y\Delta z}$$

$$\Rightarrow Z_o Z\Delta z + Z_o^2 + \frac{Z_o}{Y\Delta z} = \frac{Z_o}{Y\Delta z} + \frac{Z\Delta z}{Y\Delta z}$$

$$\Rightarrow Z_o(Z\Delta z + Z_o) = \frac{Z}{Y}$$

$$\Rightarrow Z_o Y(Z\Delta z + Z_o) = Z$$

$$\Rightarrow \lim_{\Delta z \to 0}[Z] = Z_o^2 Y$$

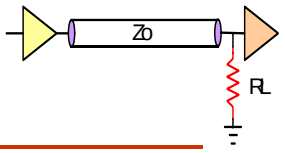
Therefore,

$$Z_o = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \qquad (2.1)$$

$$V = C/\sqrt{\varepsilon_r} \Rightarrow PD = 1/V = \sqrt{\varepsilon_r}/C$$

$$TD = \frac{x\sqrt{\varepsilon_r}}{C} \quad x = Length\ of\ line$$

$$Also \quad TD = \sqrt{LC} \quad and \quad Z_0 = \sqrt{\frac{L}{C}}$$



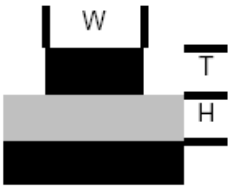
Zo for PCB Traces

Microstrip

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} Ln\left(\frac{5.98H}{.8W + T}\right)$$

$$C_0 = \frac{.67(\varepsilon_r + 1.41)}{Ln[5.98H/(.8W + T)]}$$

$$t_{pd} = 1.017\sqrt{.475\varepsilon_r + .67}$$



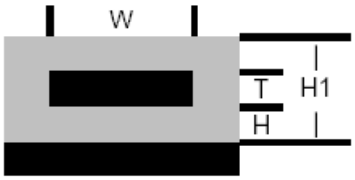
Embedded Microstrip

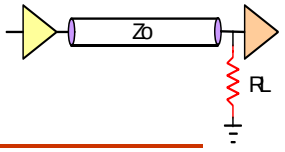
First, let: $\varepsilon_r' = \varepsilon_r\left[1 - \exp\left(\frac{-1.55H1}{H}\right)\right]$

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r'}} Ln\left(\frac{5.98H}{.8W + T}\right)$$

$$C_0 = \frac{1.41(\varepsilon_r')}{Ln[5.98H/(.8W + T)]}$$

$$t_{pd} = .08475\sqrt{\varepsilon_r'}$$





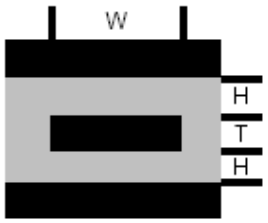
Zo for PCB Traces

Stripline

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} Ln\left(\frac{1.9(2H + T)}{(.8W + T)}\right)$$

$$C_0 = \frac{1.41\varepsilon_r}{Ln[3.81H/(.8W + T)]}$$

$$t_{pd} = 1.017\sqrt{\varepsilon_r}$$



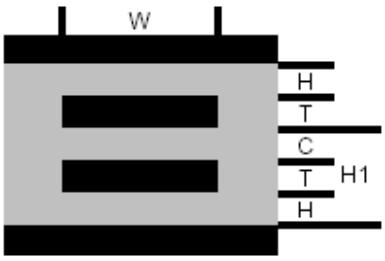
Dual or Asymmetric Stripline

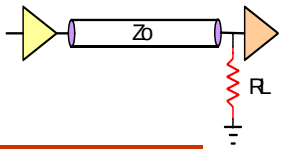
$$Z_0 = \frac{80}{\sqrt{\varepsilon_r}} Ln\left[\frac{1.9(2H + T)}{(.8W + T)}\right]\left[1 - \frac{H}{4(H1)}\right]$$

$$Z_0 = \frac{80}{\sqrt{\varepsilon_r}} Ln\left[\frac{1.9(2H + T)}{(.8W + T)}\right]\left[1 - \frac{H}{4(H + C + T)}\right]$$

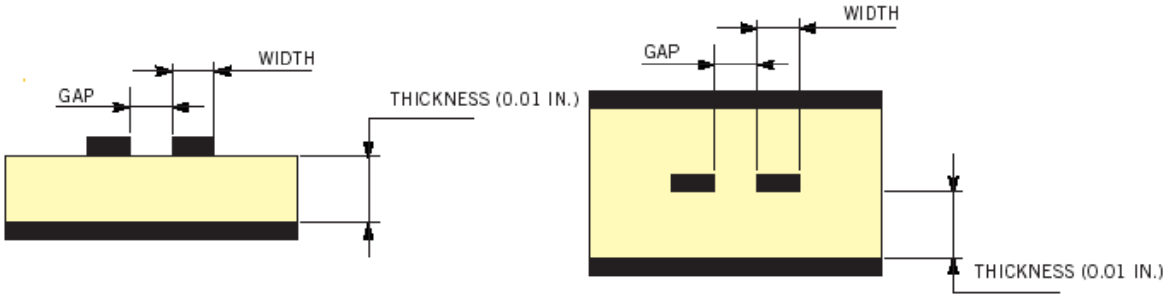
$$C_0 = \frac{2.82\varepsilon_r}{Ln[2(H - T)/(.268W + .335T)]}$$

$$t_{pd} = 1.017\sqrt{\varepsilon_r}$$



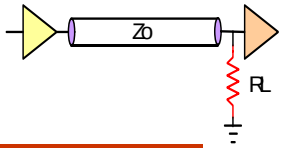


Zo for PCB Traces



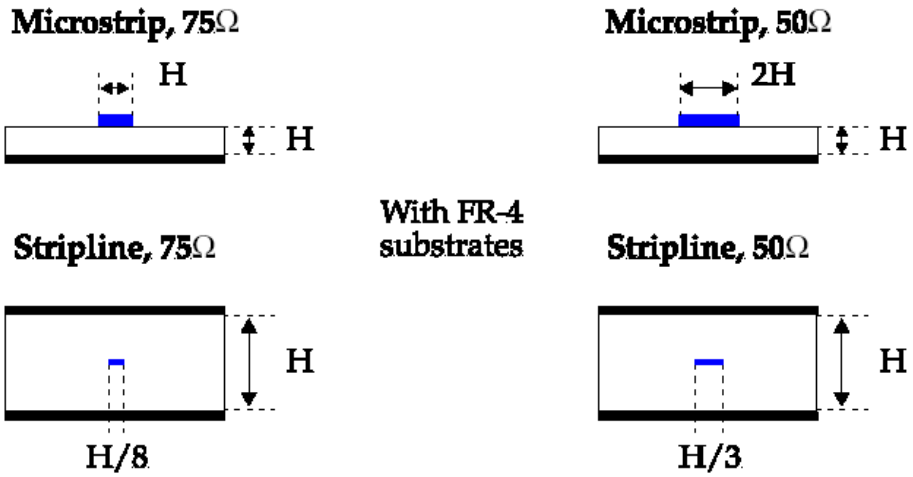
DIMENSIONS FOR 50Ω MICROSTRIP	
Gap (in.)	Width (in.)
0.005	0.011
0.01	0.0142
0.015	0.0158
0.02	0.0166
0.025	0.0171
∞	0.0185

DIMENSIONS FOR 50Ω STRIPLINE	
Gap (in.)	Width (in.)
0.005	0.0055
0.01	0.0075
0.015	0.0083
0.02	0.0086
0.025	0.0087
∞	0.0088

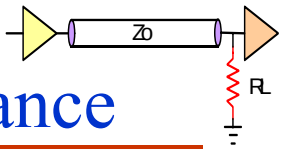


Zo for PCB Traces

The following shows the dimensions needed to build transmission lines on a PCB with characteristic impedances of 50 and 75Ωs.

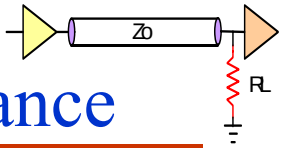


Note that the tolerance here is +/- 30%!

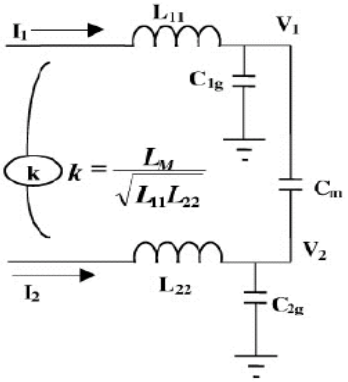


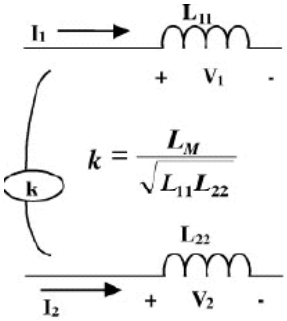
Even and Odd Mode Impedance

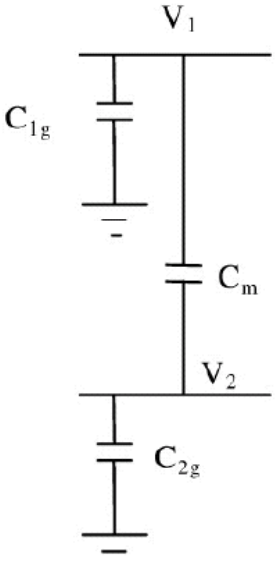
- Impedance is dependent upon switching pattern
- Odd Mode: When two coupled lines are driven with equal magnitude and 180^o out of phase.
  - Effective mutual capacitance will increase by twice the mutual capacitance
  - Equivalent inductance will decrease by mutual inductance
- Even Mode: When two coupled lines are driven with equal magnitude and in same phase.
  - Effective mutual capacitance will decrease by the mutual capacitance
  - Equivalent inductance will increase by mutual inductance



Even and Odd Mode Impedance

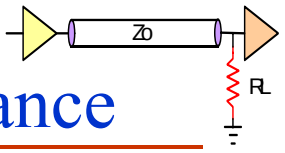






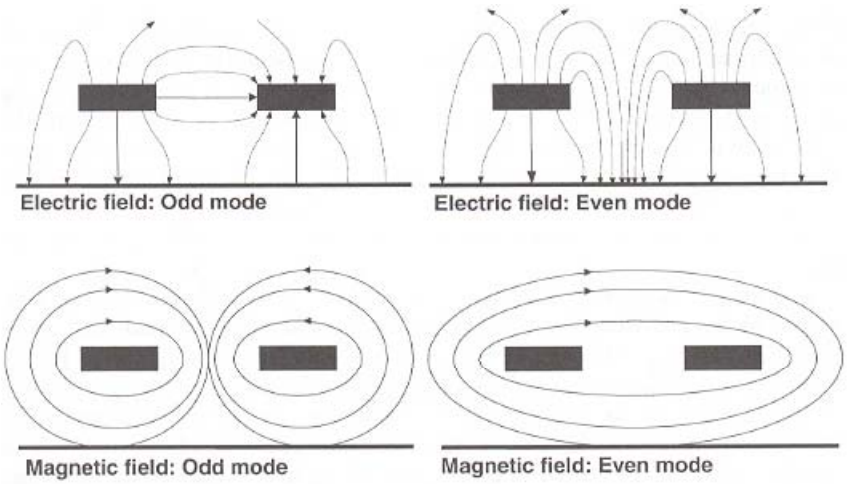
$$L_{odd} = L_{11} - L_m = L_{11} - L_{12}$$
$$C_{odd} = C_{1g} + 2C_m = C_{11} + C_{12}$$
$$Z_{odd} = \sqrt{\frac{L_{odd}}{C_{odd}}} = \sqrt{\frac{L_{11} - L_{12}}{C_{11} + C_{12}}}$$
$$TD_{odd} = \sqrt{L_{odd} C_{odd}} = \sqrt{(L_{11} - L_{12})(C_{11} + C_{12})}$$

$$L_{even} = L_{11} + L_m = L_{11} + L_{12}$$
$$C_{even} = C_{11} - C_m = C_{11} - C_{12}$$
$$Z_{even} = \sqrt{\frac{L_{even}}{C_{even}}} = \sqrt{\frac{L_{11} + L_{12}}{C_{11} - C_{12}}}$$
$$TD_{even} = \sqrt{L_{even} C_{even}} = \sqrt{(L_{11} + L_{12})(C_{11} - C_{12})}$$

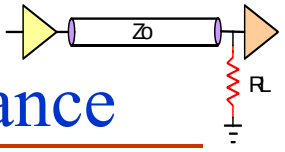


Even and Odd Mode Impedance

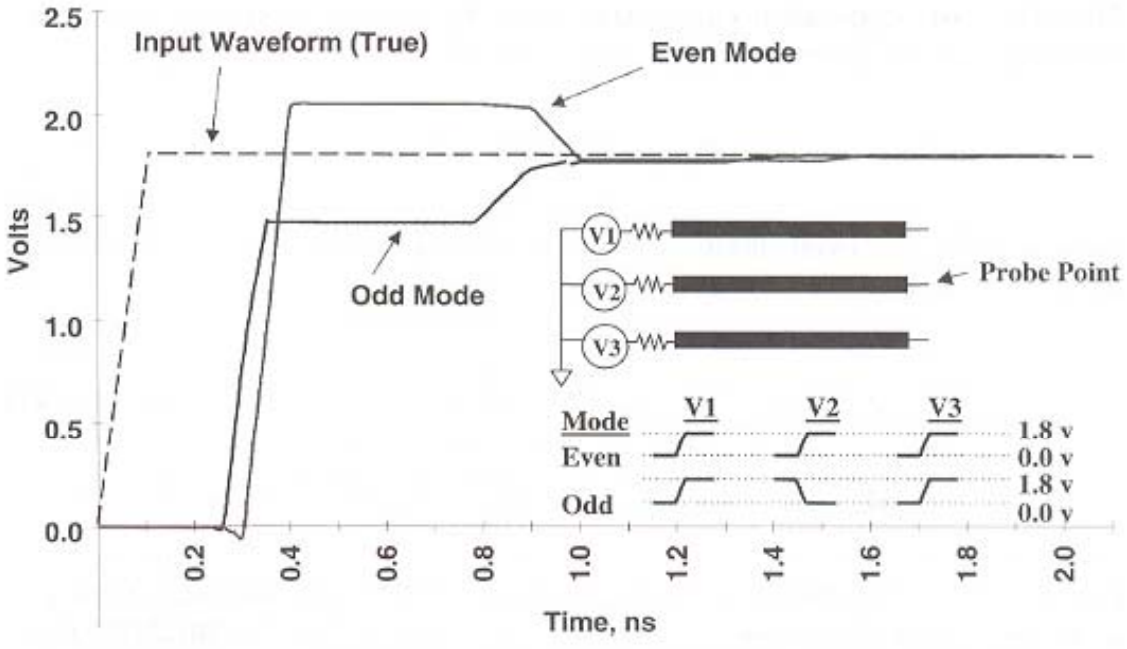
- Odd mode Zo will be lower than single line case.
- Even mode Zo will be higher than the single line case.
- There is velocity variation due to crosstalk in microstrip but not in stripline



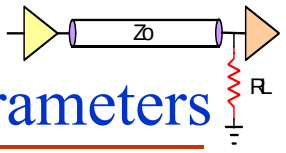
Odd- and even-mode electric and magnetic field patterns for a simple two-conductor system.



Even and Odd Mode Impedance



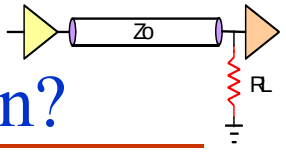
Effect of switching patterns on a three-conductor system.



Dependence of Zo on Different Parameters

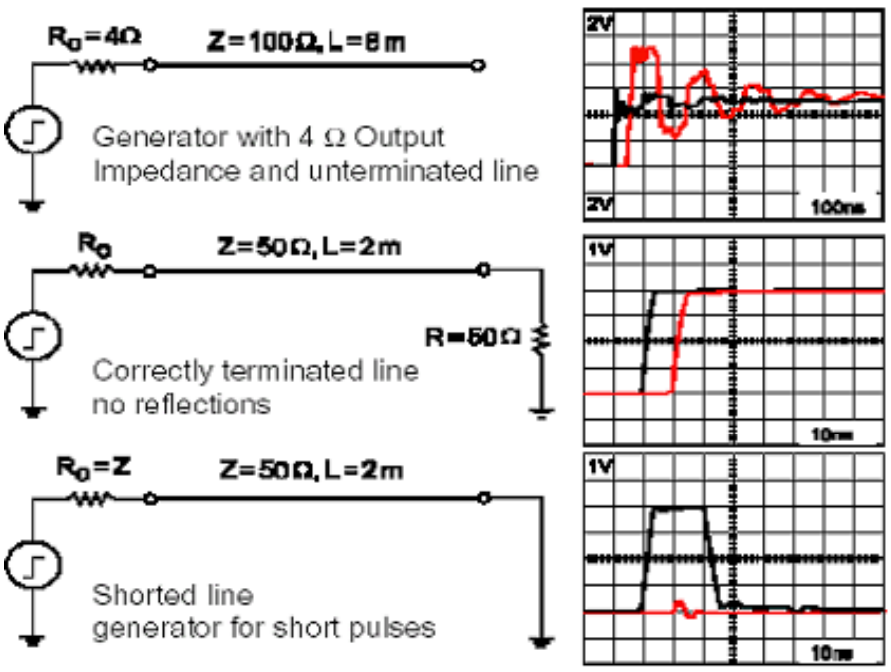
PARAMETER	NOMINAL VALUE	3σ VARIATION	3σ Z0
Line width	0.005″	10%	2.5Ω
Dielectric thickness	0.005″	10%	1.5 Ω
Dk	0.0045″	5%	0.75Ω
Soldermask thickness	0.0004″	10%	0.5Ω
Trace thickness	0.0012″	20%	0.5Ω
Copper height of surface traces	0.0022″	30%	0.5Ω
Dk of material between the traces	0.0035″	10%	0.5Ω
Top to foot width difference	0.0008″	10%	0.2Ω
Soldermask Dk	0.0044″	10%	0.2Ω
Edge-to-edge separation	0.015″	5%	0.1Ω

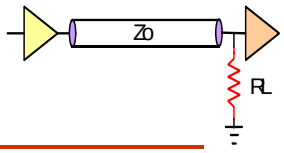
Based on characteristic impedance for 0.005"-wide traces in stripline and microstrip. Note: The variations in impedance typically add as RMS. Not all these terms would apply to the same specific line.



When we need Termination?

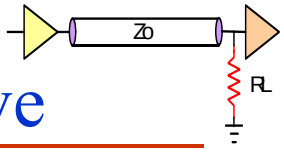
- When length of trace is more than 1/8th of electrical length of rising edge.
- The trace (cable) is short and drives the heavy capacitive load, there is possibility of ringing



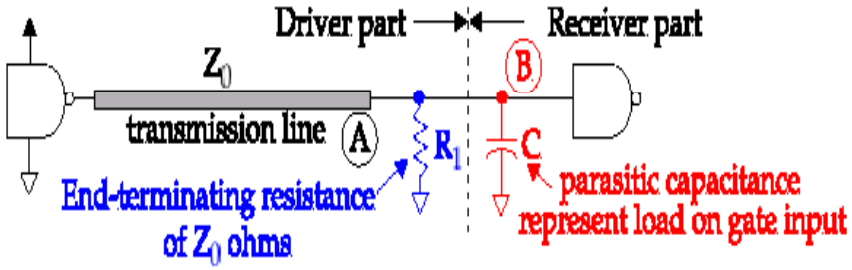


Types of terminations

- End Terminations
  - Resistive
  - Split Resistive
  - AC Biased
  - Diode Termination
- Series Terminations
  - Source Series



End Termination: Resistive

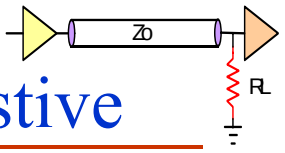


$$\tau = \frac{Z_o}{2} C$$

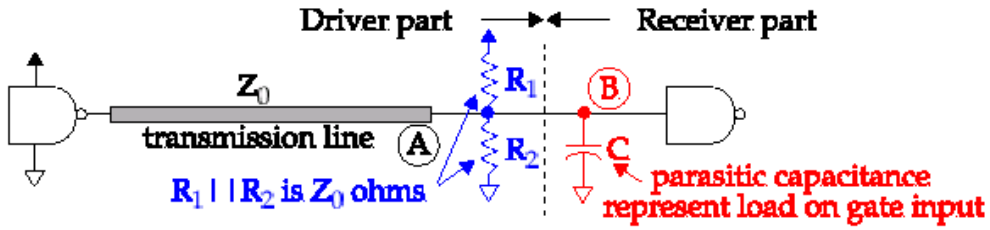
previously

$$\tau_{10-90\%} = 1.1 Z_o C$$

- Characteristics of Far End Termination
  - The Driving waveform propagates at full intensity to receiver.
  - All Reflection are damped by terminating resistors.
  - The received voltage is equal to transmitted voltage
- Drawback
  - The driver must supply VCC/R_1 to terminating resistor.
  - For TTL in high state I= 5V/50Ω =100mA ; Just imagine the 64 bit BUS !!
  - This termination scheme rarely appears in TTL, LVTTL and CMOS circuits



End Termination: Split Resistive

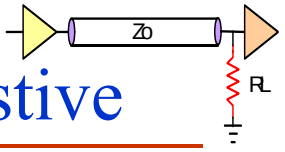


- The load of heavy current is lifted off the driver.
- R1 and R2 should be chosen such that it do not exceed the I_{OHmax} and I_{OLmax} limits of driving gate.
- For R2>R1, low current exceeds high current.

$$Y_1 = \frac{1}{R_1} \; and \; Y_2 = \frac{1}{R_2}$$

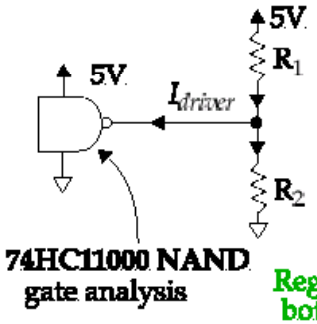
$$\Rightarrow Y_1 + Y_2 = \frac{1}{Z_o}$$

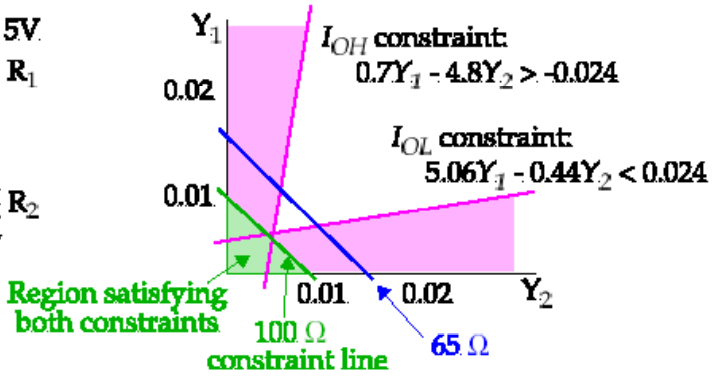
$$V_{ter\,min\,ate} = \frac{R_1 V_{EE} + R_2 V_{CC}}{R_1 + R_2}$$



End Termination: Split Resistive

- R1=R2 Good for HCMOS
- R2>R1 Good for TTL and CMOS

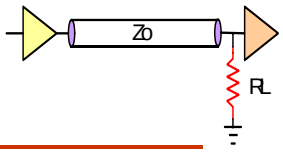




- All valid combination of R_1 and R_2 lies on the green and blue line.

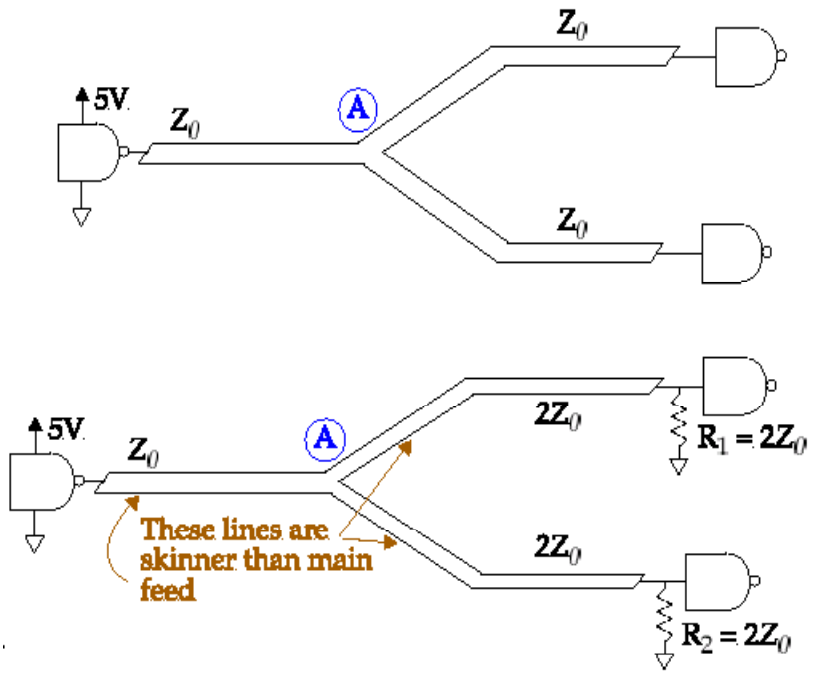
$$(V_{CC} - V_{OH})Y_1 - (V_{OH} - V_{EE})Y_2 > I_{OHmax}$$
$$(V_{CC} - V_{OL})Y_1 - (V_{OL} - V_{EE})Y_2 < I_{OLmax}$$

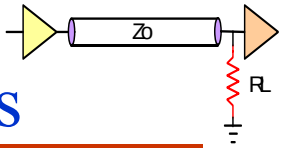
- The 100Ω line passes the constraint limit and shows the values of R1 and R2 be 100Ω each.
- The 65Ω line do not satisfy the constraints limit at any point.
- Driver can't drive 65 Ohms.



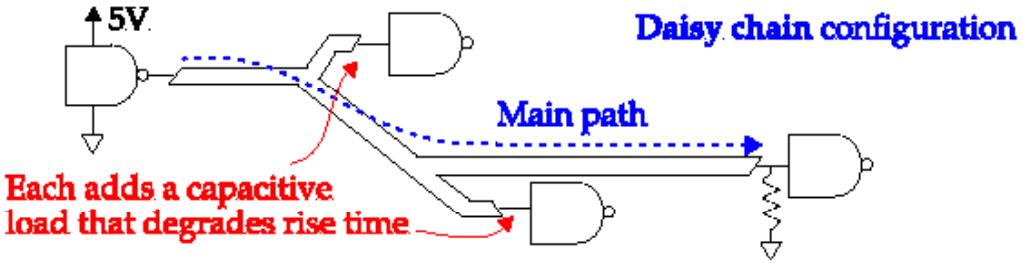
Bifurcated Lines

- There will reflection from point A.
- Bottom figure solves the problem, Not used due to problems in fabrication.

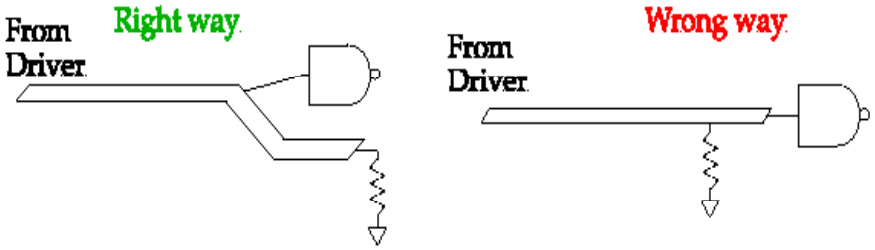


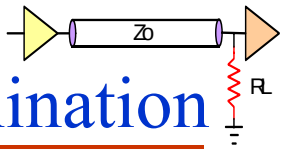


Multiple Bifurcated Lines



- End termination allows receiver to be placed at any point along the line.
- Keep the connecting stubs short compared to length of rising edge to avoid reflection and bifurcation points.

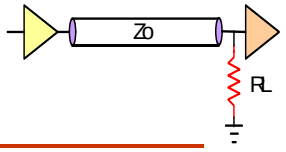




Power Dissipation in End Termination

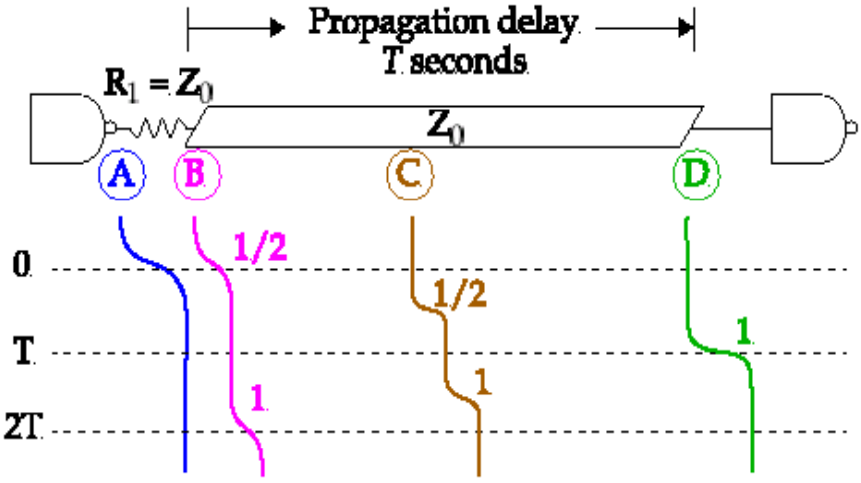
- Load dissipation is inversely proportional to termination impedance.
- Also depends upon high and low operating voltages.
- Under assumption that equal time is spend in Low and High states.

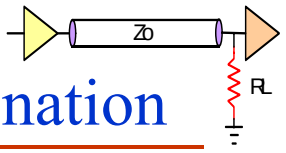
$$P_{load} = \left[\frac{(V_{HI} - V_{EE})^2 + (V_{LO} - V_{EE})^2}{2R_2} + \frac{(V_{CC} - V_{HI})^2 + (V_{CC} - V_{LO})^2}{2R_1} \right]$$



Source Termination

- Characteristics of Source Termination
  - The drive waveform is cut half before it starts propagating.
  - The driving signal propagates at HALF the intensity toward end.
  - At the far end the signal reflects (+1, open circuit) with same intensity.
  - This restores the signal in full intensity.
  - This signal propagates back and damps at the source termination.





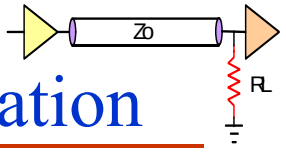
Resistance value at Source Termination

- Drivers have very small output impedance i.e ECL~10Ω in both low and high states. TTL, LVTTL and CMOS both have different impedance for Logic 1 and 0.
- **Driver Impedance + Source Termination Impedance = Z_o.**
- The source terminating impedance is typically less than Z_o.
- So for TTL, LVTTL and CMOS its compromise between both values.
- For capacitive load the RC time constant

$$\tau = Z_o C \Rightarrow \tau_{10-90\%} = 2.2 Z_o C$$

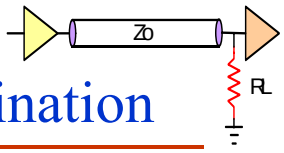
$$previously \quad \tau_{10-90\%} = 1.1 Z_o C$$

- **Rise time is twice than End Terminated case with same transmission line impedance as load.**



Advantage of Source Termination

- It is easier to eliminate reflection at the source than at far end of transmission line in digital circuits.
- While the source has resistive output load (plus a little inductance), the receiver usually has a capacitive load which is usually more difficult to match.
- This is especially true when driving multiple loads.
- Therefore the ***reflection coefficient*** at the driver is more nearly zero than the coefficient at the receiver under end termination.
- ***This gives the more overall flatter response.***



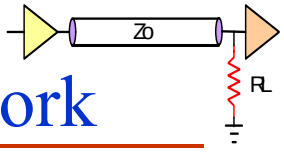
Power Requirement by Source Termination

- The worse current drive lasts only for round trip line delay.
- The source termination resistor has voltage of *ΔV/2* impressed it during the entire round trip delay *2T* after switching.
- Energy Dissipated in resistor

$$E = 2T\left(\frac{\Delta V}{2}\right)^2 \frac{1}{R} \quad \because \Delta V \text{ is diffrence between High \& Low}$$

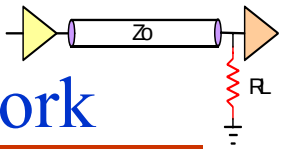
$$\Rightarrow Power \approx \frac{(PulseFrequency)T\Delta V^2}{2R}$$

- This amount of Power is less than power dissipated in End Termination



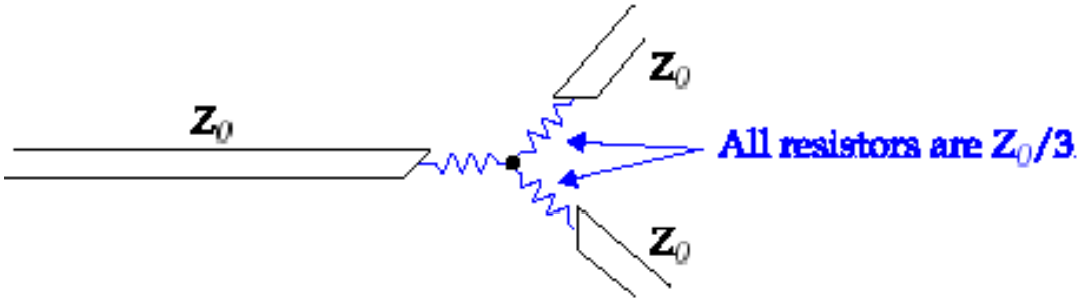
Connecting Hair-Ball Network

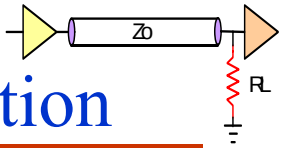
- Four Approaches.
  - Add source termination to every driver.
    - Takes little power, provides a little bit of damping and reduces settling time.
  - Add an end termination to each driver.
    - Lot of power and works well in star configuration, reflection are confined to source and middle star point.
  - Add shunt termination in middle.
    - Stupid Configuration, looses the impedance of central point.



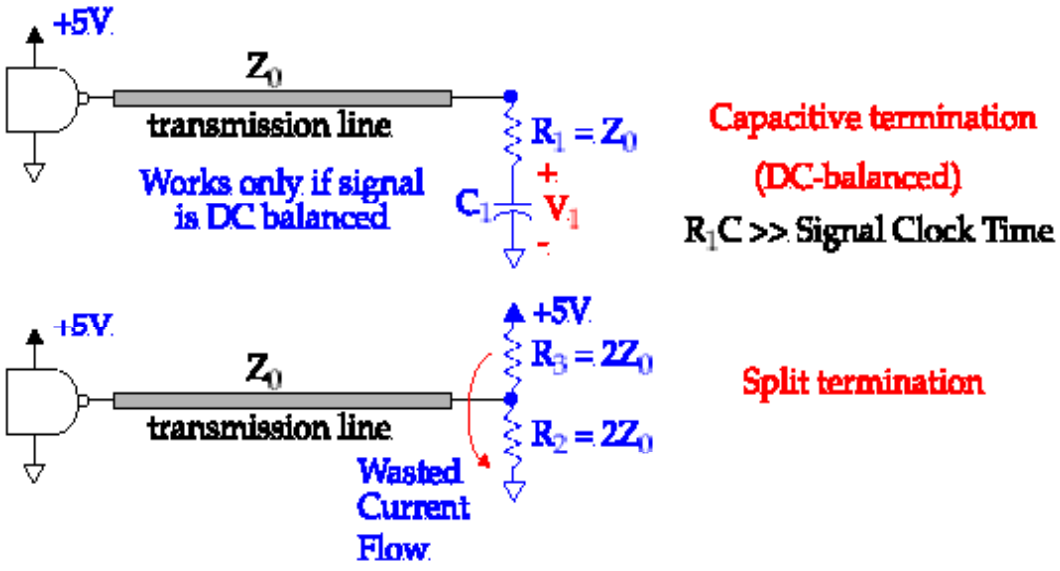
Connecting Hair-Ball Network

– Add series resistance between every junction of the branches.
  - Attenuates the signal at every Junction.
  - Middle Termination can improve system step response only at expense of signal attenuation.

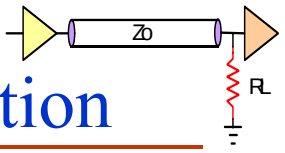




AC Biasing of End Termination



- Capacitors reduces Quiescent power dissipation.



AC Biasing of End Termination

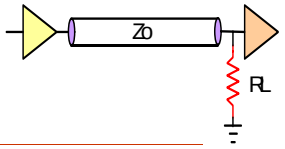
- Twice the power in burned in case with out capacitor.

$$P_{R1} = \frac{\left(\Delta V/2\right)^2}{Z_o} = \Delta V^2/4Z_0 \quad \because \Delta V \text{ is diffrence between High \& Low}$$

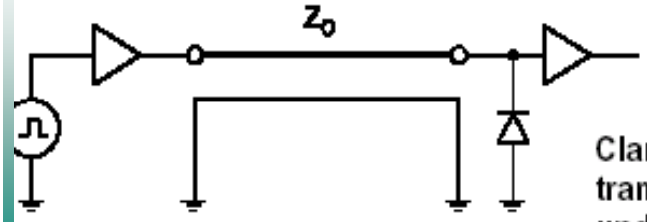
While split resistors

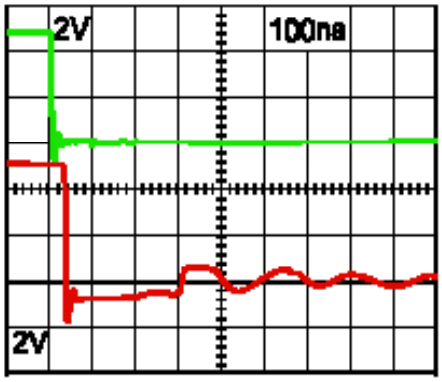
$$P_{R2+R3} = \frac{(\Delta V)^2}{2Z_o}$$

- From perspective of driver, the two terminations are same only dissipation in termination resistors differ.



Diode Termination

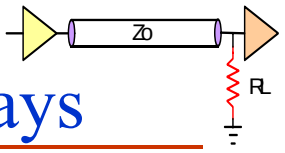




Clamping diodes at the end of the transmission line absorbe the energy of under- and overshoots and ensure a clean signal waveform.
Input circuits of logic ICs contain these clamping diodes.

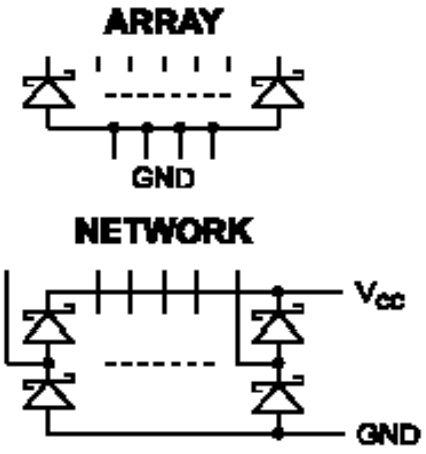
Note: The clamping diodes of VLSI circuits are often not capable to handle the high currents generated by line reflections (parasitic transistors!). Provide additional Schottly clamping diodes!

Schottky Diode Arrays:
SN74S1050, SN74S1051, SN74S1052, SN74S1053, SN74S1056, SN74F1056, SN74F1016, SN74F1018



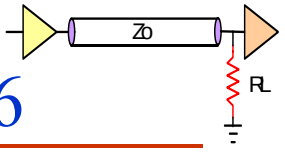
Bus termination Diode Arrays

Released Functions :
SN74S1050 12-Bit Schottky Diode Array
SN74S1051 12-Bit Schottky Diode Network
SN74S1052 16-Bit Schottky Diode Array
SN74S1053 16-Bit Schottky Diode Network
SN74S1056 8-Bit Schottky Diode Array
SN74F1056 9-Bit Schottky Diode Array
SN74F1016 16-Bit Schottky Diode
R-C Bus Termination Array
SN74F1018 18-Bit Schottky Diode
R-C Bus Termination Array

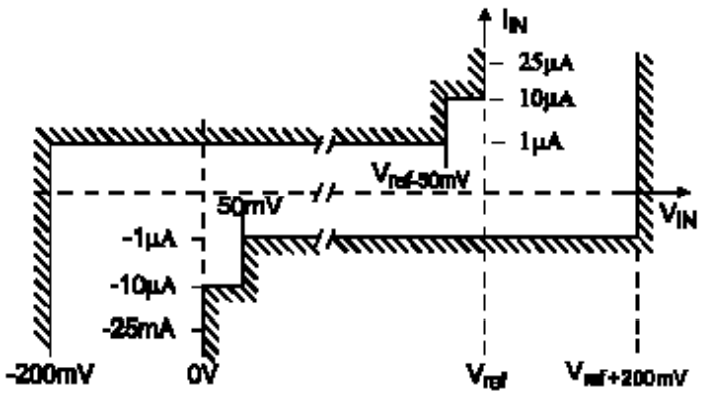


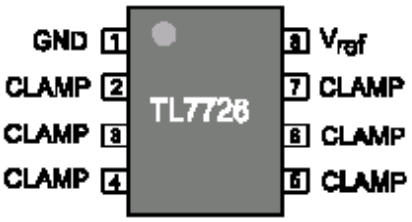
Applications :

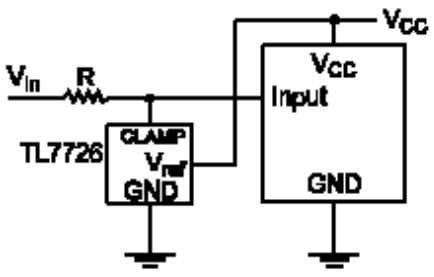
- ★Arrays in TTL systems
- ★Networks in CMOS systems (positive overshoots)
- ★Small buses, e.g. Memory Arrays
- ★System bus in personal computers



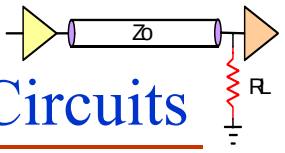
Clamping Circuit TL7326





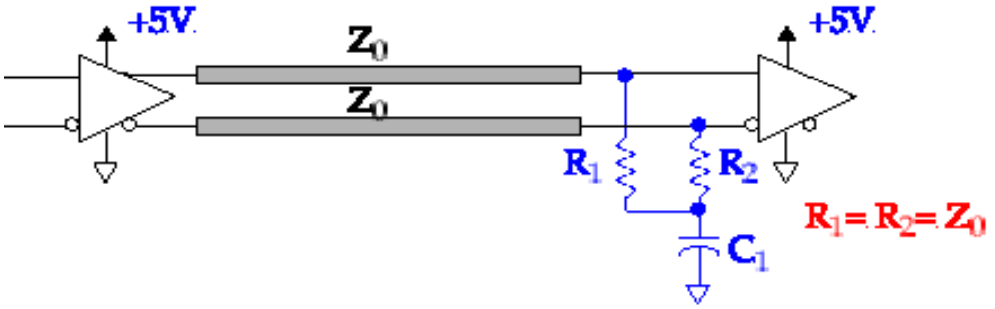


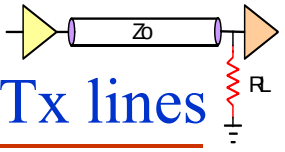
★The clamping circuit TL7726 protects sensitive analog and digital inputs against excessive overvoltages and by that ensures the function of the circuit.



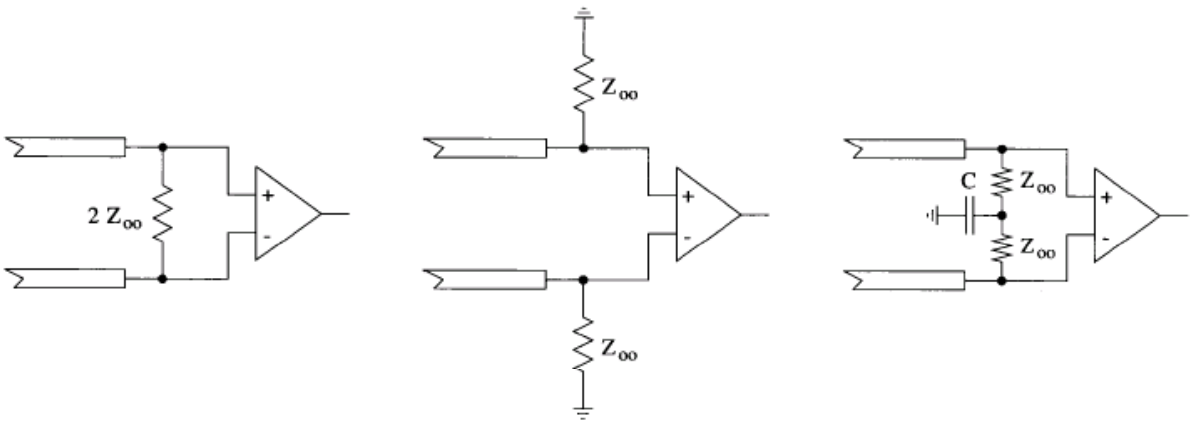
End Termination for Differential Circuits

- Combination of RC circuit terminates DC-Balanced lines with no wasted quiescent power.

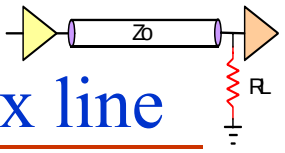




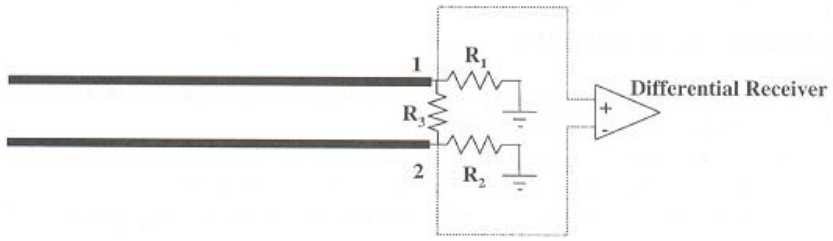
Imperfect Termination for Coupled Tx lines



Imperfect termination for a differential transmission line pair: (a) bridged, (b) single-ended (c) AC.



PI Termination for Coupled Tx line

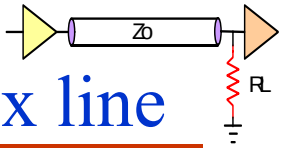


Pi termination configuration for a coupled transmission line pair.

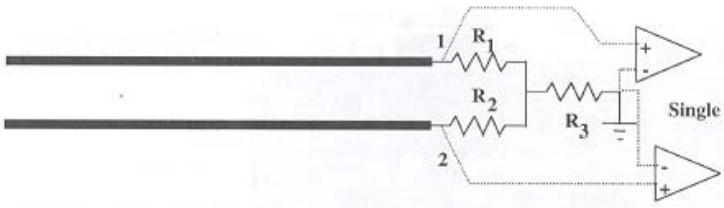
$$R_1 = R_2 = Z_{even}$$

$$R_3 = \frac{2Z_{even}Z_{odd}}{Z_{even} - Z_{odd}}$$

Equivalent of termination seen in the odd mode with the pi termination configuration.



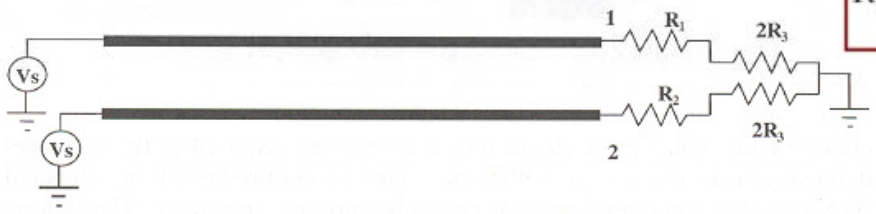
T- Termination for Coupled Tx line



T termination configuration for a coupled transmission line pair.

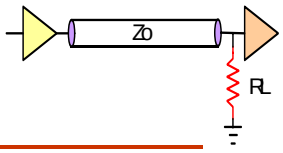
$$R_1 = R_2 = Z_{odd}$$

$$R_3 = \frac{1}{2}\left(Z_{even} - Z_{odd}\right)$$



Equivalent of termination seen in the even mode with the T termination configuration.

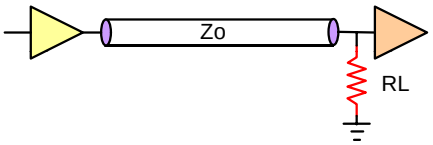
Termination: Summery



Parallel

Pros: Terminate to either Gnd or Vcc
R easy to determine
Only one additional component
Performs well with distributed loads

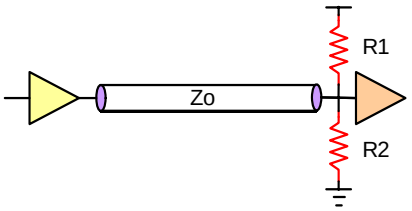
Cons: Power dissipated in R_L at all times
Power requirement high



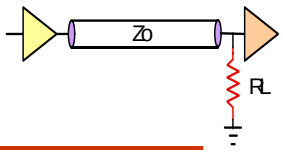
Thevenin

Pros: Properly chosen, pull up/down resisters can improve noise margins
Performs well with distributed loads

Cons: Results in steady flow of current through R's
Optimumselection of R_1 and R_2 can be complicated
Complicated if used with tri-state devices



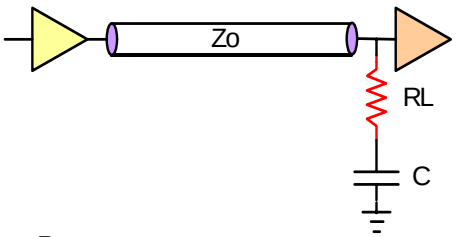
Termination: Summery



AC

Pros: Performs as well as parallel without the dc power drain

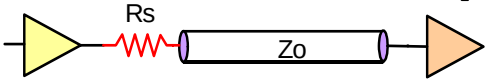
Cons: C is difficult to optimize
Requires 2 components
Can lead to timing problems



Series

Pros: One component
No dc load

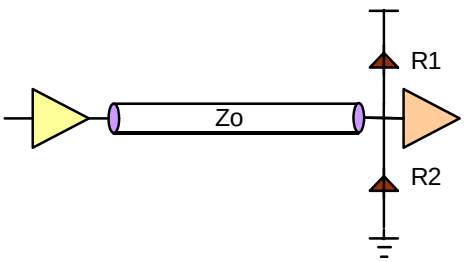
Cons: Can be difficult to optimize R_S
There IS a reverse reflection.

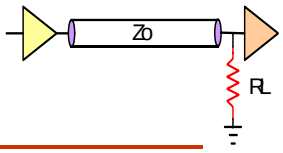


Diode

Pros: Does not depend on Zo
Little increase in power
Can be placed anywhere on line

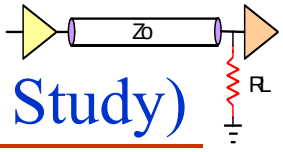
Cons: Reflections still exist
Requires 2 devices
Diodes must be FAST with low foreword voltage



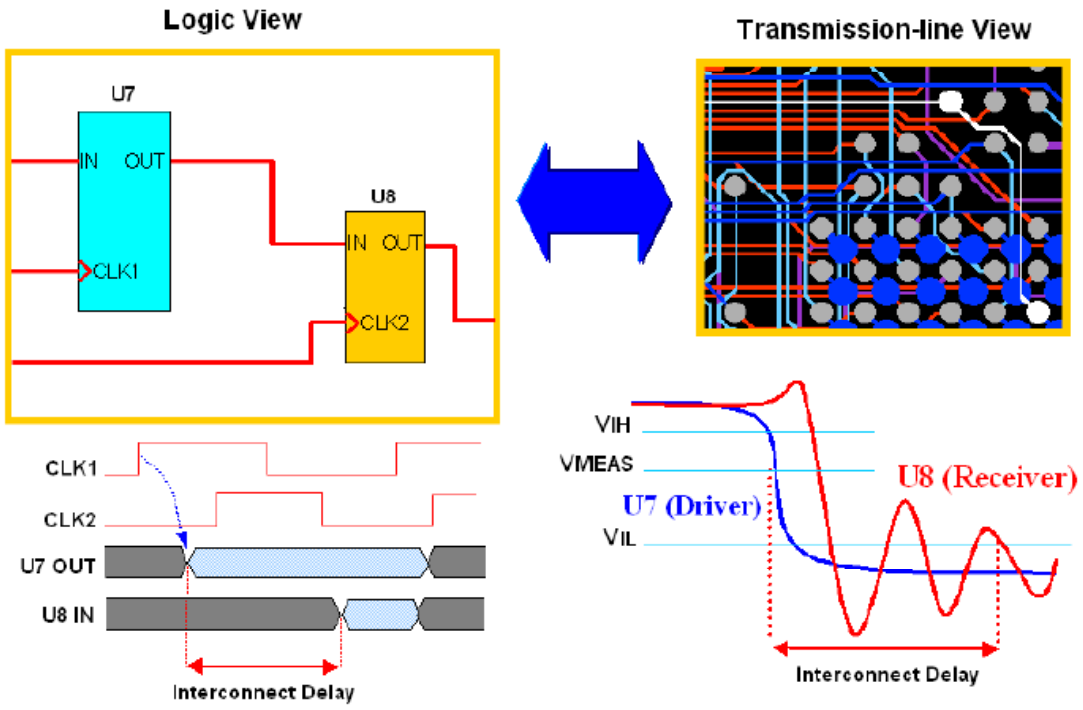


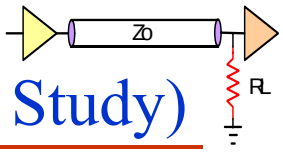
Termination: Summery

Details	Logic Level	Power	Speed
End Termination Parallel	Good	Bad (Static Power)	Good (Next Switching at time T)
Source Series	Good	Good (Dynamic Power)	Bad (Next Switching at time 2T)



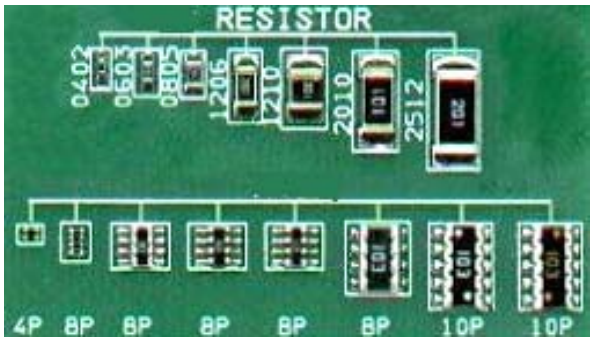
Clock and Bus Termination (Case Study)

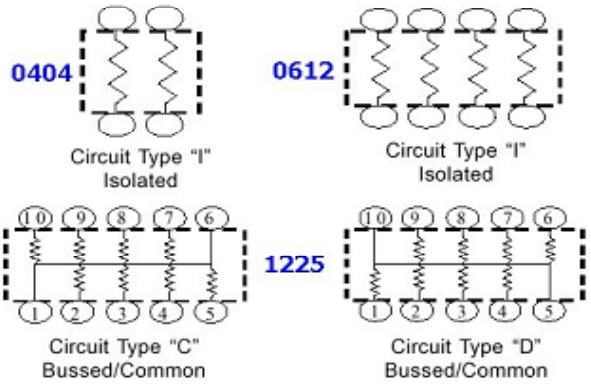


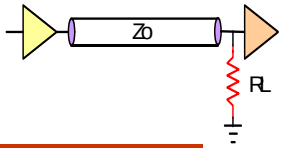


Clock and Bus Termination (Case Study)

- Board Designed by Rashad.M.Ramzan
- CLK Speed 350 MHz
- Bus Speed 110 MHz
- Bus Width 32 Bits (**View in Altium**)

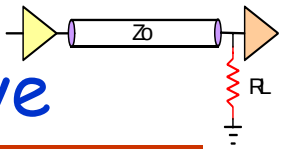




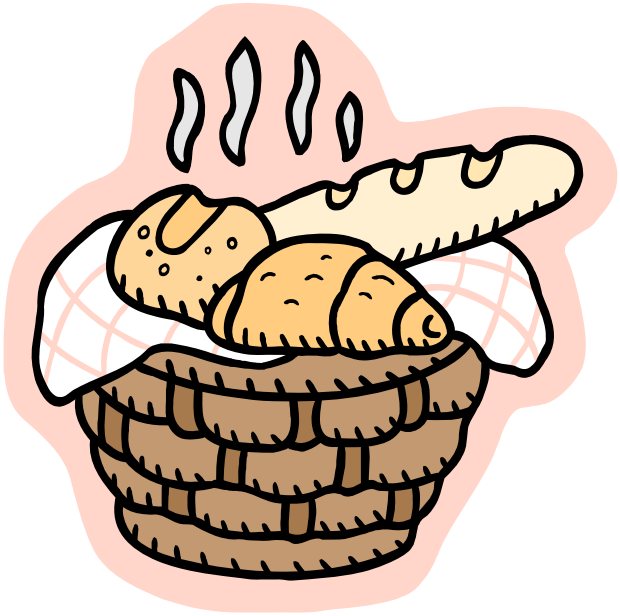


Summary

- Impedance
  - Why Zo is important?
  - Basic Definition and Concept
  - Impedance Formula (Dependence on Geometry)
    - Stripline, Microstrip, Embedded Stripline, Embedded Microstrip
  - Even and Odd mode Impedance
- Termination
  - When termination is ndded
  - Types of Termination
    - End Termination, Split Termination, Series and Diode Termination
    - AC biasing
    - Termination of Coupled Differential Lines (Even and Odd Mode Impedance)
  - CASE STUDY (CLK and Bus Termination)



Wakeup Please lets have Some Food….



45