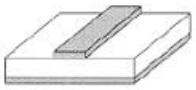
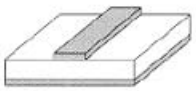


Power Distribution,Decoupling Plane Stack-up and Grounding

Rashad.M.Ramzan, Ph.D

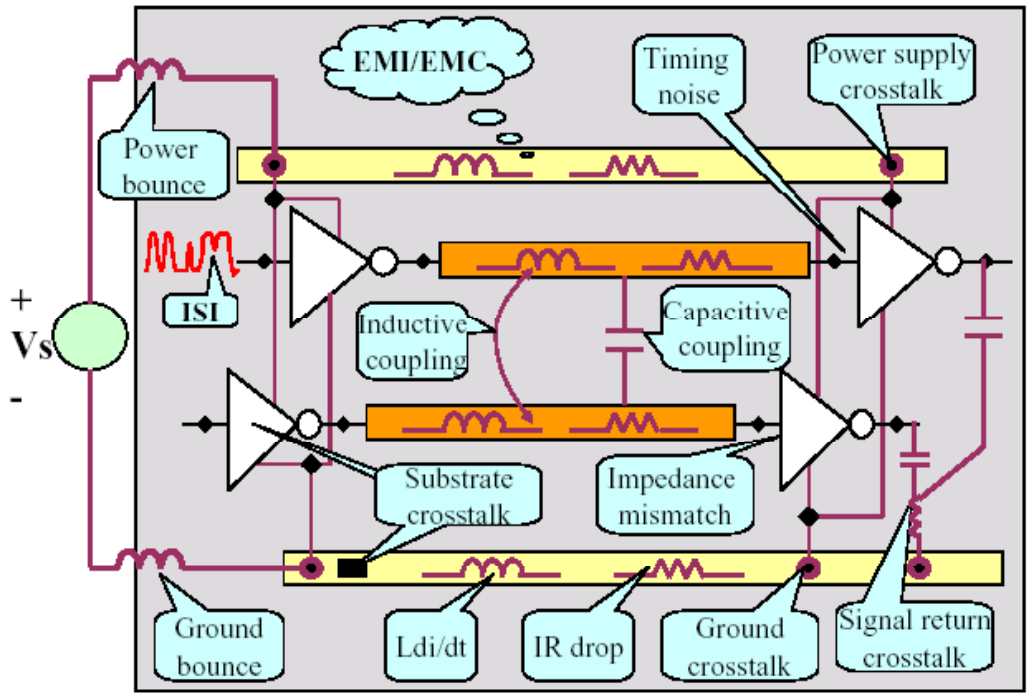
FAST-NU, Islamabad



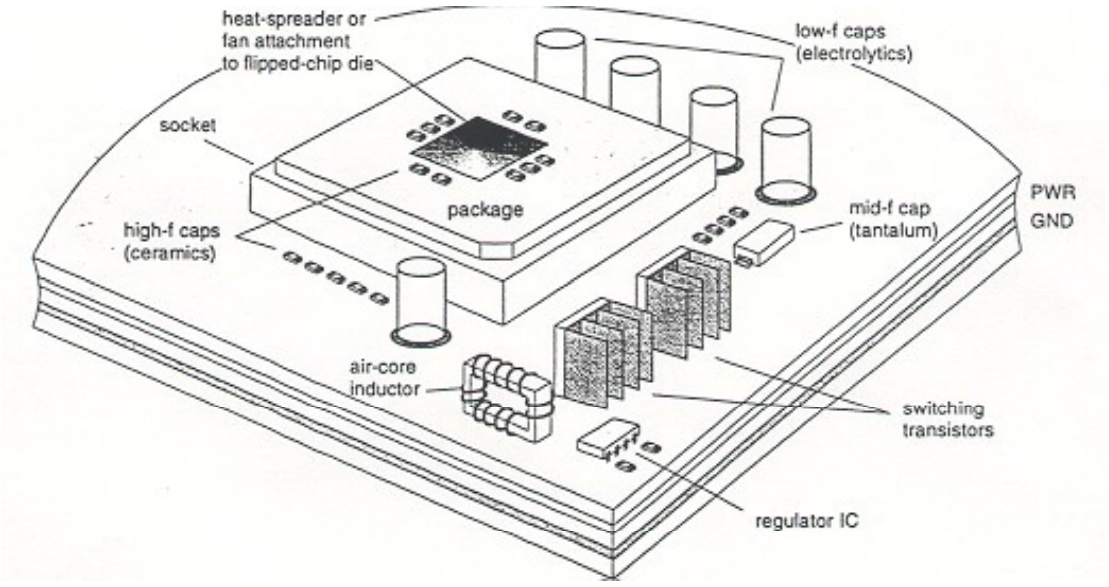
Today's Topics

- Power Distribution
  - Power Line Resistance
  - Power Line Inductance
- Power Planes
  - Decoupling Capacitors
  - PWR-GND Plane as Decoupling Capacitor
  - Layer Stack Up
  - Split Planes
- Grounding Techniques
  - One Point Grounding
  - Grounding for Mixed signal ICs
  - Slots in Ground Planes

Noise: Cumulative Overview

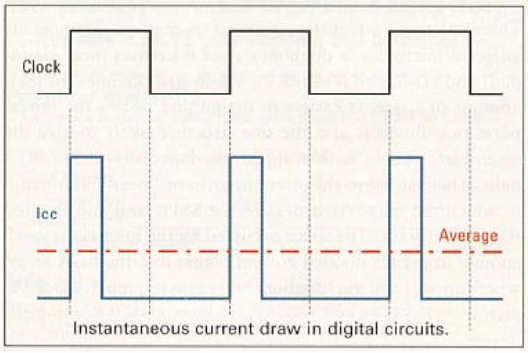


Elements of Power Distribution



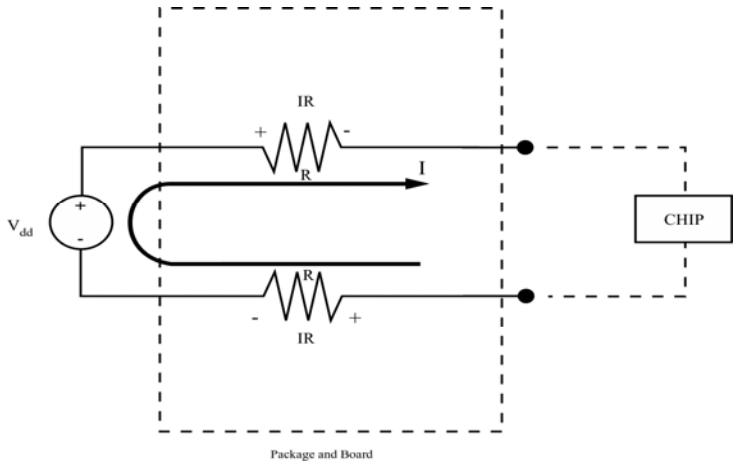
Ref: Dennis Herrell and Benjamin Beker, “Modeling of Power Distribution Systems in PCs”, pp. 159 – 162, EPEP ’98.

Typical Digital Circuit



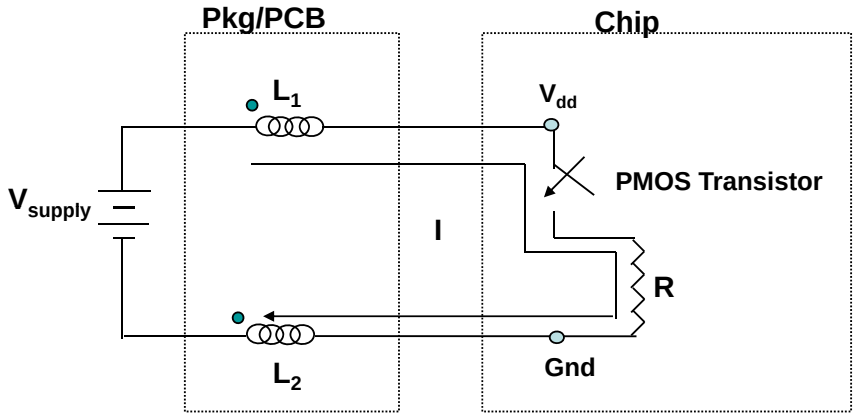
- Typically in 100Mhz Digital device with average current of 4A, actual current may exceed 20 A in first few ns of clock cycle.
- We can't effort 20 A supply??
- Other Factors
  - Supply(VCC. GND) Trace Resistance
  - Supply(VCC. GND) Trace Inductance

Resistive Drop



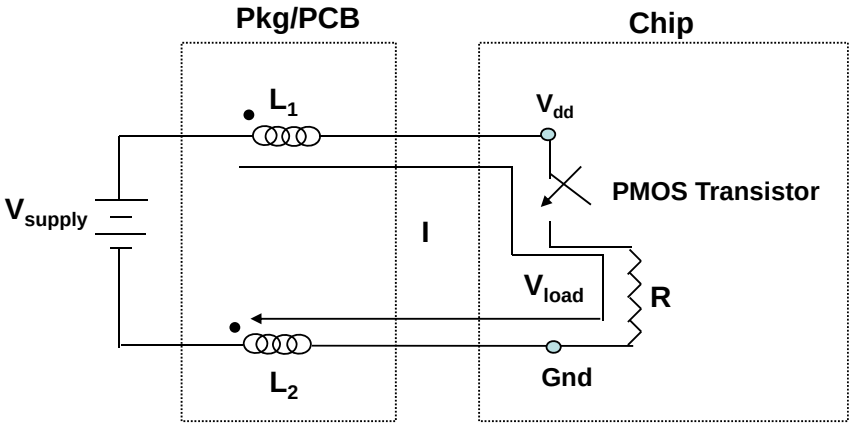
- DC current flows to the chip
- PCB and Package metallization have DC resistance
- Current flows from Vdd into Gnd
- Causes voltage drop IR

Inductive Drop



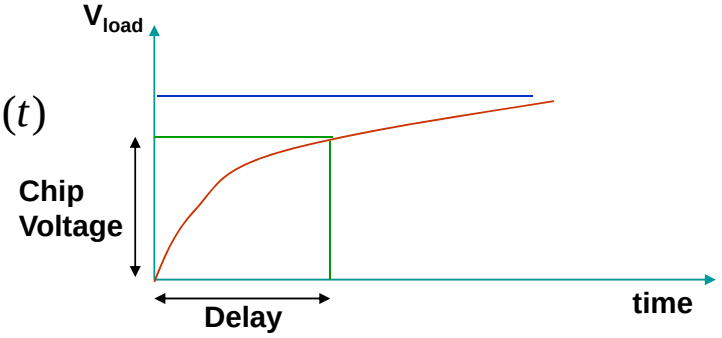
- All physical connections contain inductance
- Vsupply is on the corner of the PCB
- L1 and L2 are the package and PCB inductances
- Chip is a switch (as discussed earlier)

Inductive Effect



$$V_{load}(t) = V_{sup\,ply}(1 - e^{-t/\tau})u(t)$$

$$\tau = \frac{L_1 + L_2}{R}$$

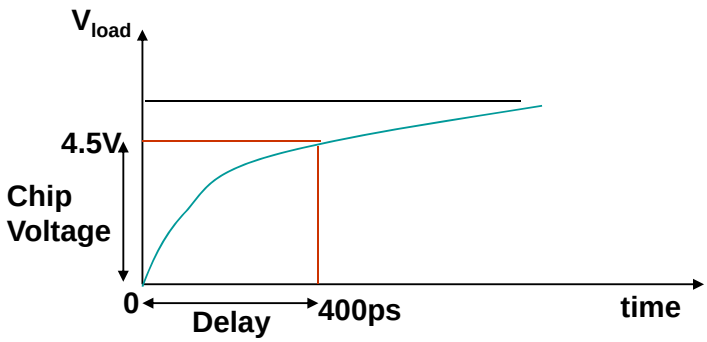


Inductive Effect – An Example

$$V_{load}(t) = V_{sup\,ply}(1 - e^{-t/\tau})u(t) \qquad \tau = \frac{L_1 + L_2}{R}$$

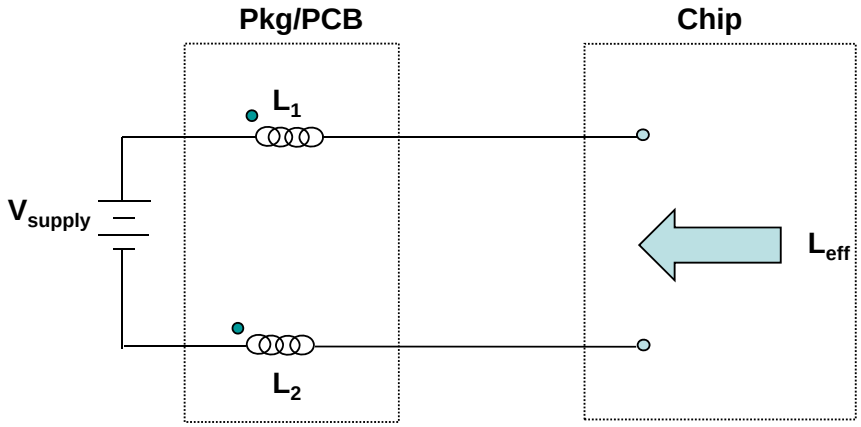
For V_{supply} = 5V, R = 50Ω , L_1 = 1nH , L_2 = 1nH

$$\tau = 40\,ps$$



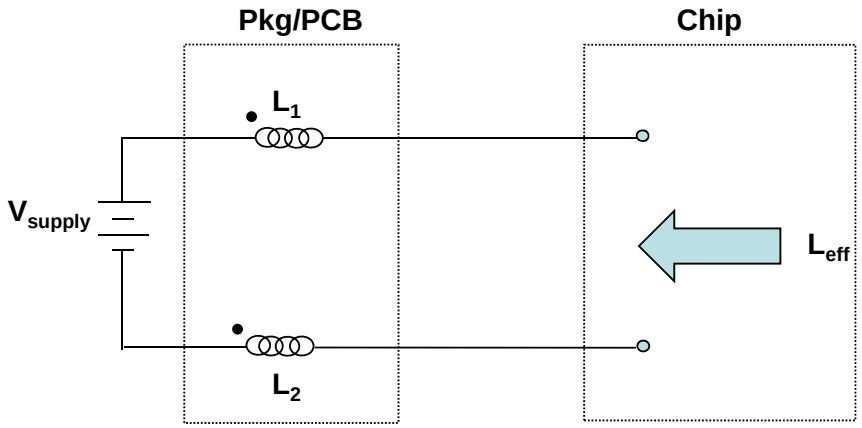
- Chip voltage rises slowly
- Requires 400ps to reach 4.5V
- Causes delay in the circuit
- Due to the inductive effect

Effective Inductance



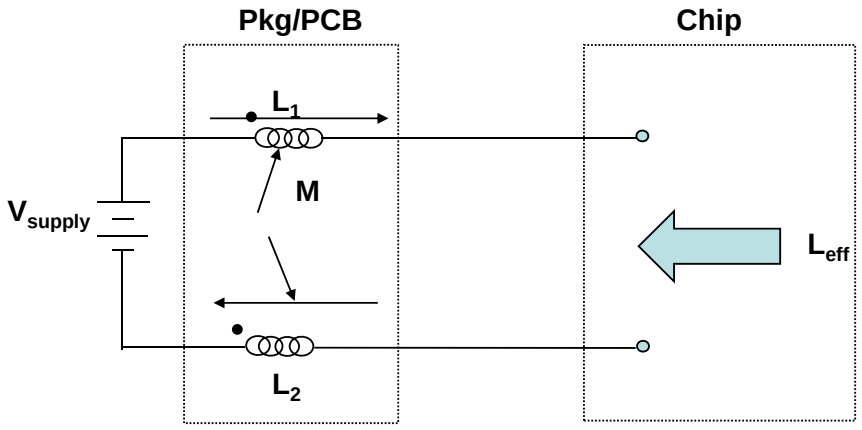
- L_{eff} is the effective inductance for the current loop
- It is the inductance seen by the chip
- $L_{eff} = L_1 + L_2$

Effective Inductance



- L_1 and L_2 are the inductances of the voltage and ground connections
- Physical proximity of connections causes a mutual inductance
- Based on the direction of current in the inductors, the mutual inductance contribution to L_{eff} can be either additive or subtractive
- For voltage and ground connections, mutual inductance has a subtractive effect

Effective Inductance - Example



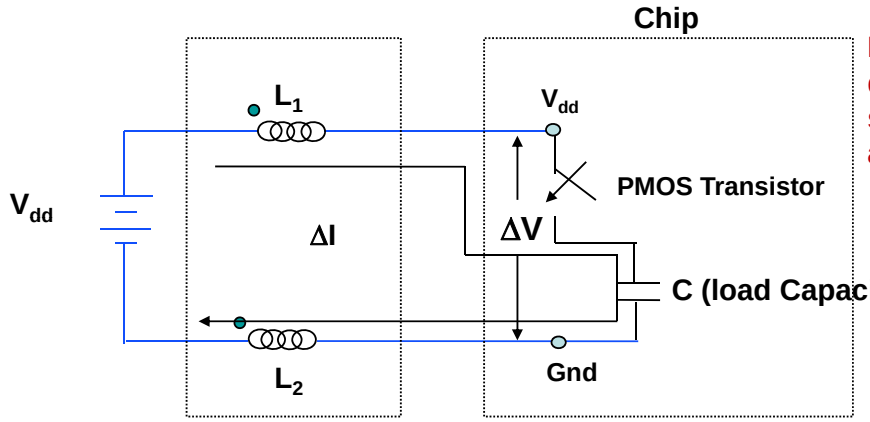
For V_{supply} = 5V, R = 50Ω , L_1 = 1nH , L_2 = 1nH, M=0.5nH

$$\tau = 20\,ps$$

$L_{eff} = L_1 + L_2 - 2M$ = 1nH

• Voltage and ground connections (via, planes…) should have large mutual inductance between them to reduce the effective inductance of the circuit

Supply Noise - Inside IC



Noise produced due to logic gate switching within a chip

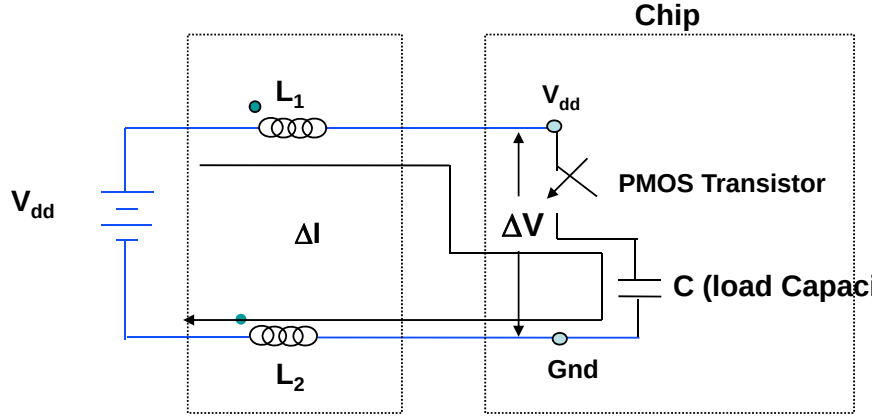
$Q = CV_{dd}$ **Charge required to charge the load capacitor**

$\Delta I = C\ V_{dd}/\Delta t$ **Supplied by a change in current in the circuit**

$\Delta I_{total} = NC\ V_{dd}/\Delta t$ **Current change for N gates**

$$L_{eff} \le \frac{\Delta V(\Delta t)^2}{NCV_{dd}}$$ **Acceptable L_{eff} for the Core**

Supply Noise - Inside IC

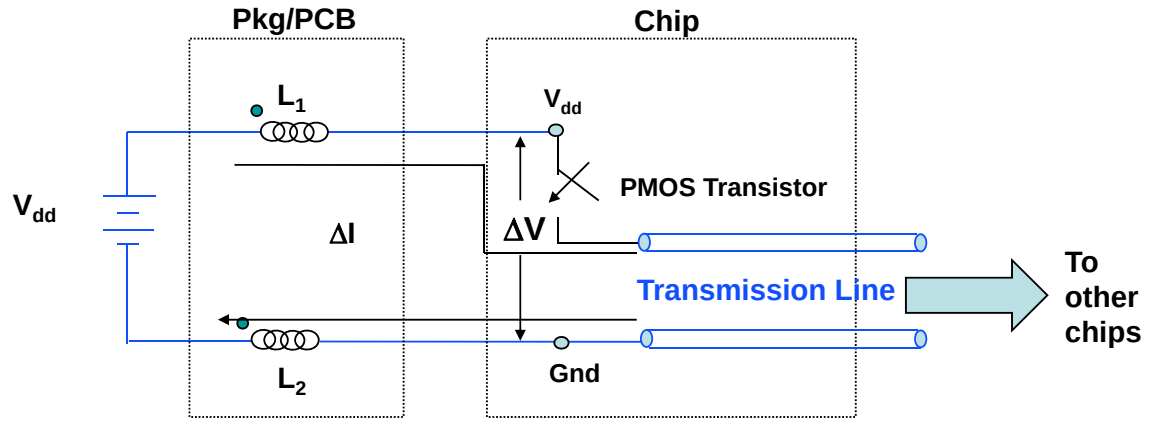


C = 1pF ; ΔV = 10%V_{dd} ; Switching time = 100ps ; Logic gates = 1000

$$L_{eff} \le \frac{\Delta V(\Delta t)^2}{NCV_{dd}}$$

Effective inductance desired = 1pH !!!!!

Supply Noise - PCB



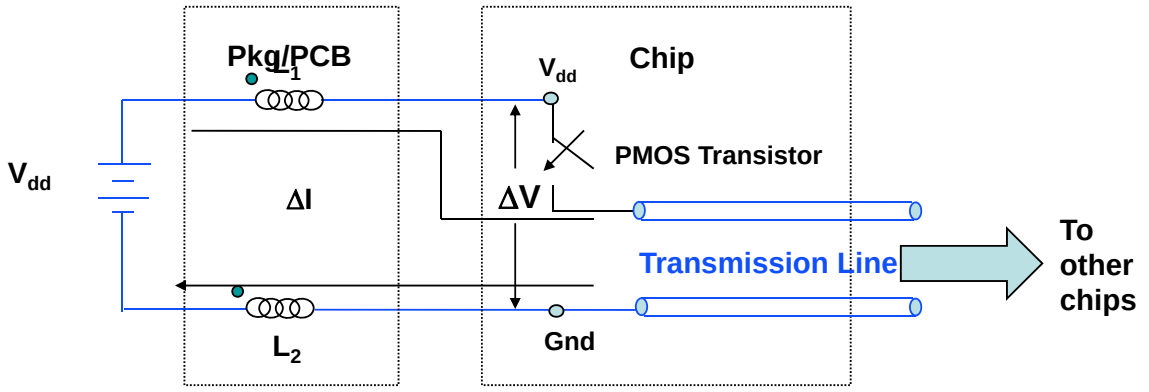
$I = V/Z_0$ **Current launched on the transmission line (forward wave)**

$\Delta I = \frac{V_{dd}}{Z0}$ **Current drawn from the supply**

$\Delta I_{total} = N\frac{V_{dd}}{Z0}$ **Current drawn for N transmission lines**

$$L_{eff} \le \frac{\Delta V Z_0}{N\frac{V_{dd}}{\Delta t}}$$ **Acceptable L_{eff} for the I/O**

Supply Noise - PCB



N = 64 (bit wide bus) ; ΔV = 10%V_{dd} ; Switching time = 1ns ; Z_0 = 50Ω

$$L_{eff} \le \frac{\Delta V Z_0}{N\frac{V_{dd}}{\Delta t}}$$

Effective inductance desired = 78pH, Impossible!!!

Target Impedance Trends

- Target impedance is falling ~1.6X, every 3 years

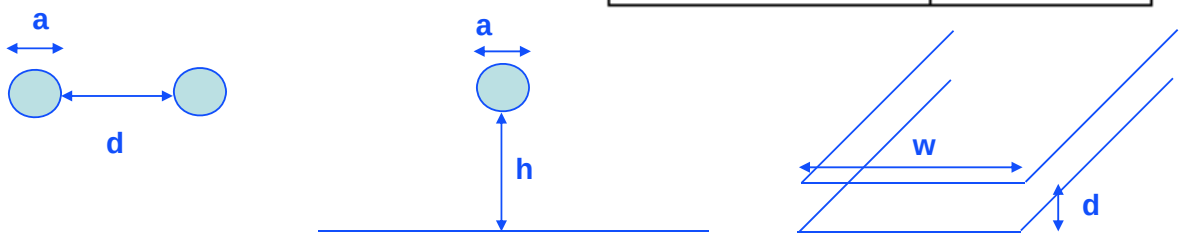
$$Z_{target} = \frac{(Power\_Supply\_Voltage)\times(Allowed\_Ripple)}{Maximum\_Current} = \frac{2.5V \times 5\%}{40.3amp} = 3.1m\Omega$$

Year of first production	1997	1999	2002	2005	2008
Chip technology	0.25um	0.18um	0.13um	0.10um	0.07um
Across Chip Frequency (MHz)	450	600	800	1000	1100
Max. Chip Power (W)	100	120	140	160	180
Max current (A)	40.3	66.7	93.3	133.3	180.0
Power Supply (V)	2.5	1.8	1.5	1.2	0.9
Target Impedance (mΩ)	3.1	1.3	0.8	0.45	0.25

What To Do?

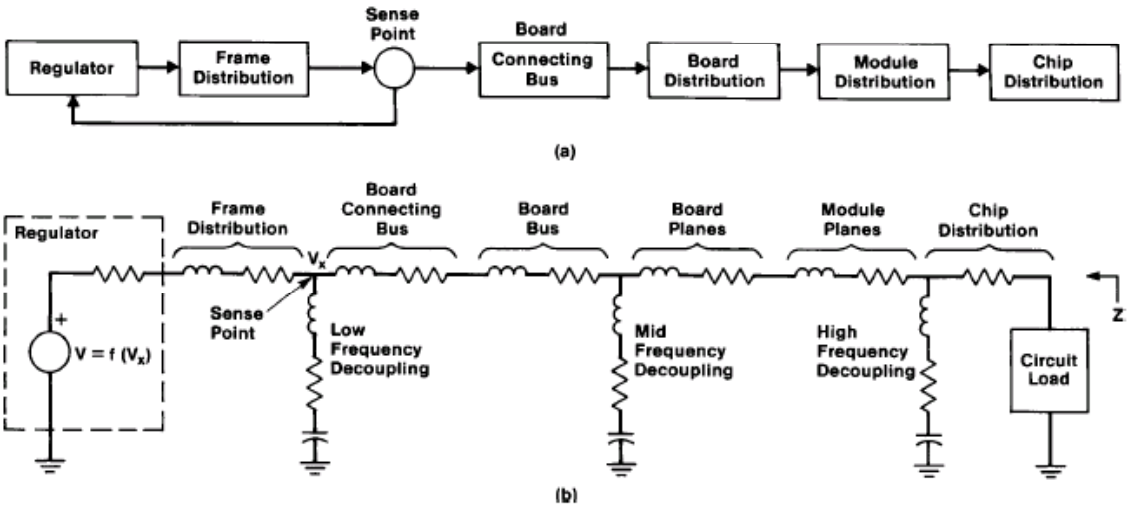
- Want to Reduce the Resistance & Inductance of Power Supply Network?
- Solution
  - Decoupling capacitor
  - Power and GND Planes

Structure	Inductance
Parallel Wires	3 - 50nH
Wire above ground plane	1 - 10nH
Parallel Planes	0.25 - 1nH



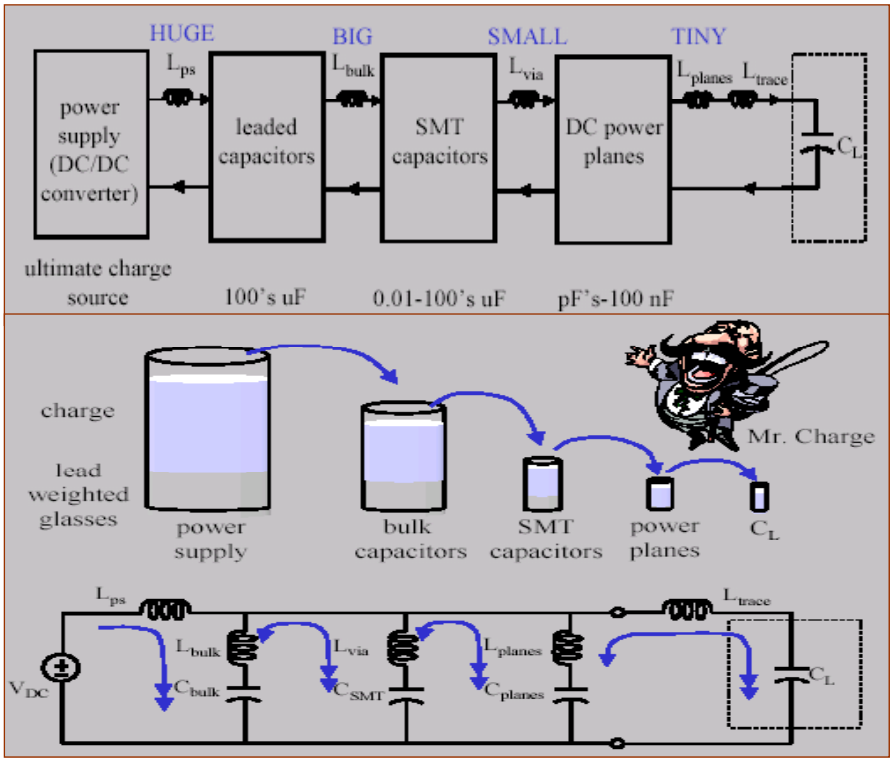
Parallel Wires **Wire above plane** **Parallel Planes**

System Supply Design

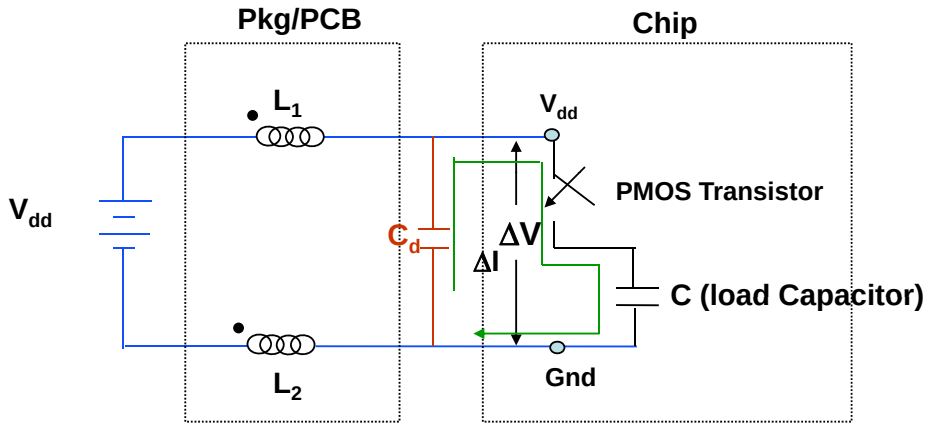


Chip power supply noise is very much dependent on packaging. Chip-packaging co-design is needed for a good PDS design.

Typical Board Decoupling

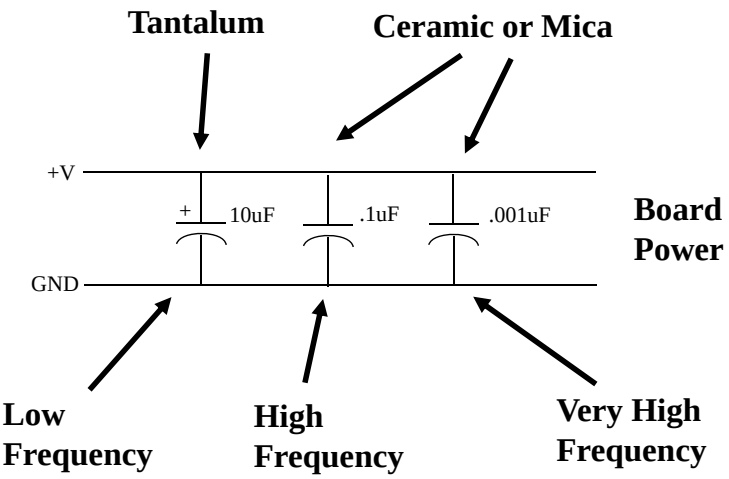


Decoupling Capacitor



- Charge Q is required to charge the load
- This results in a current change ΔI in the loop
- This is supplies by the decoupling capacitor C_d
- Capacitor therefore reduces the size of the current loop thereby reducing ΔV

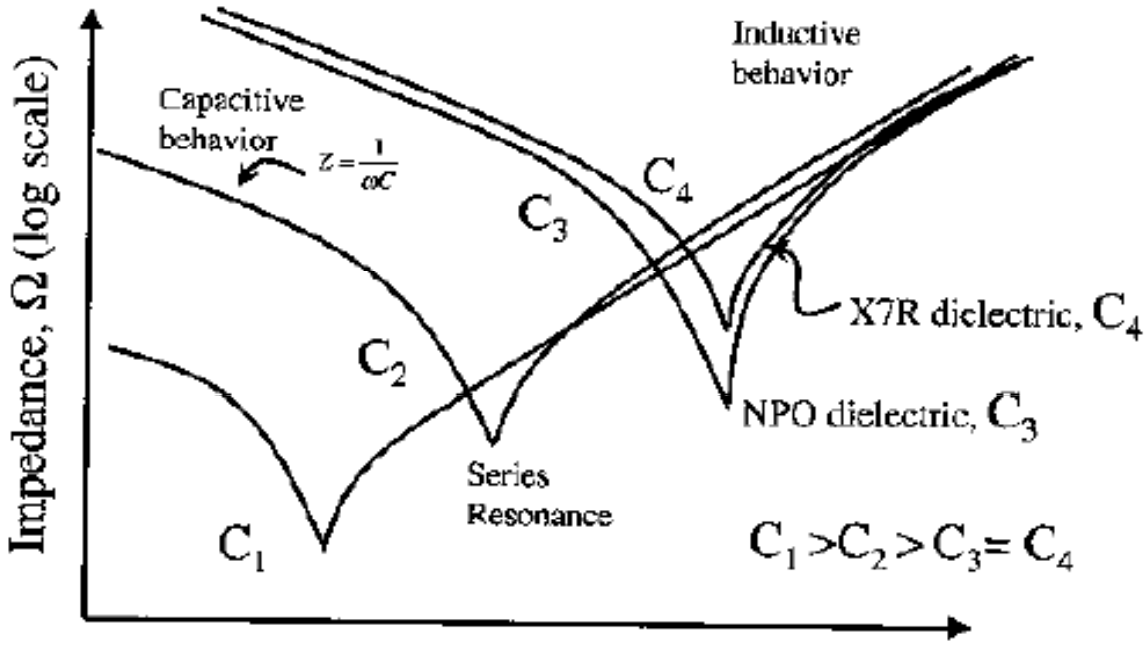
Typical Board Decoupling



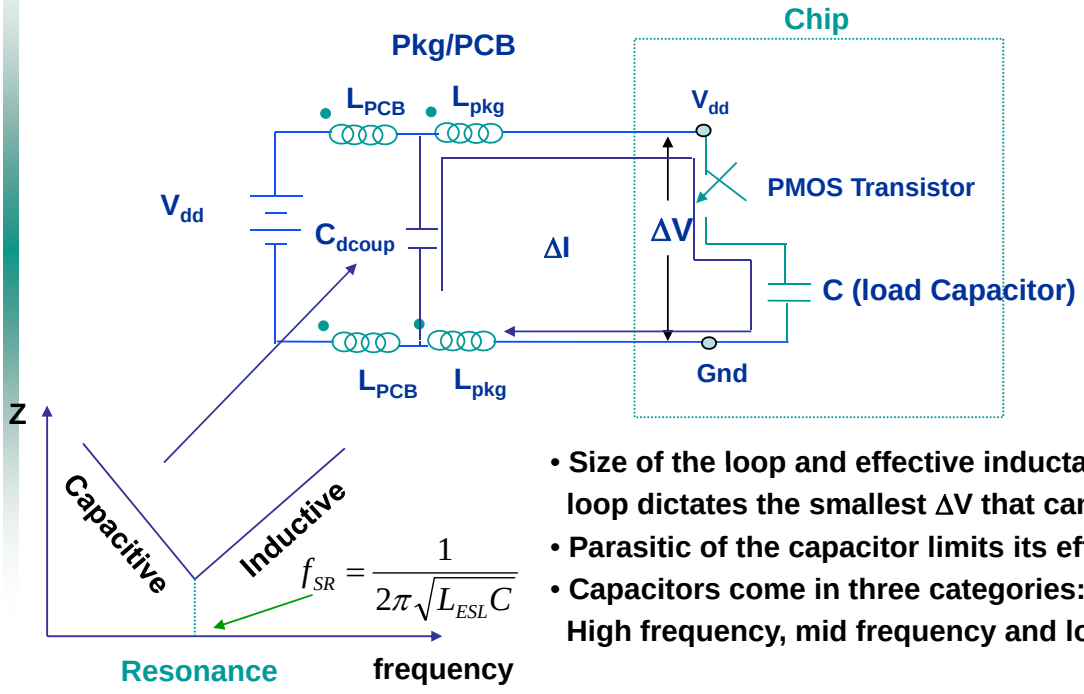
A PC mother board with board level by-pass filter (use parallel capacitors to make a big one: reduce leg inductance; save size and cost

Low ESR 0.1uf and .001uf Capacitors with IC

Total Impedence



Effectiveness of Decoupling Capacitor

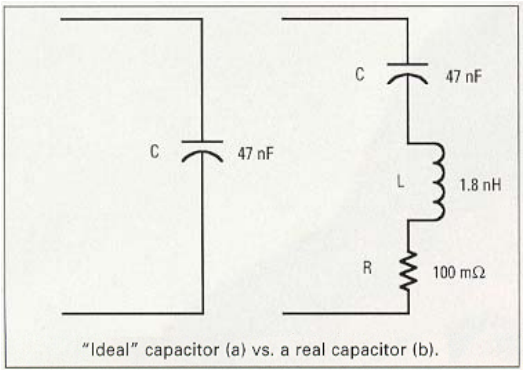


- Size of the loop and effective inductance in the loop dictates the smallest ΔV that can be achieved
- Parasitic of the capacitor limits its effectiveness
- Capacitors come in three categories: High frequency, mid frequency and low frequency

Capacitor becomes inductive past the resonant frequency

Ideal vs. Real Capacitor

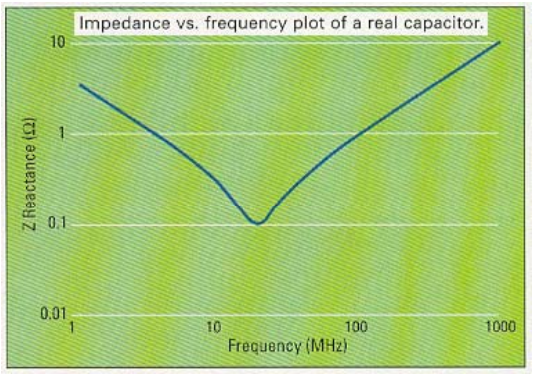
- ESR: Effective Series resistance
- ESL: Effective Series Inductance



"Ideal" capacitor (a) vs. a real capacitor (b).

ESL Values for Various Capacitor Packages

PACKAGE SIZE	ESL min (nH)	ESL max (nH)
0402	0.54	1.90
0603	0.54	1.95
0805	0.70	1.94
1206	1.37	2.26
1210	0.61	1.55
1812	0.91	2.25
1815	0.98	1.96
Radial Package	6.0	15.0
Axial Package	12.0	20.0



Design Guide Lines Below 500MHz

On boards with closely spaced power and ground planes:

the location of the decoupling capacitors is not critical

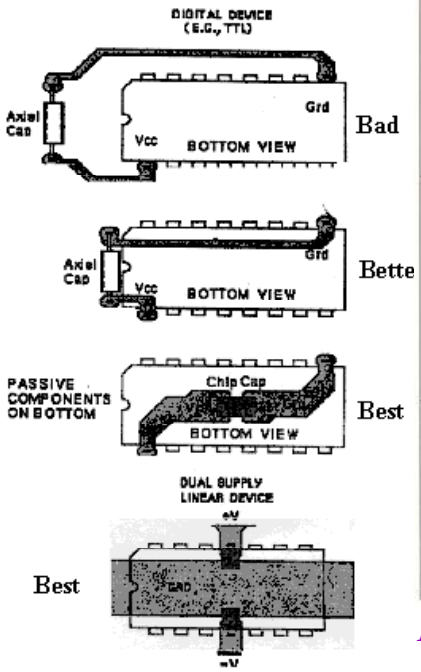
the value of the local decoupling capacitors is not critical, but it must be greater than the interplane capacitance

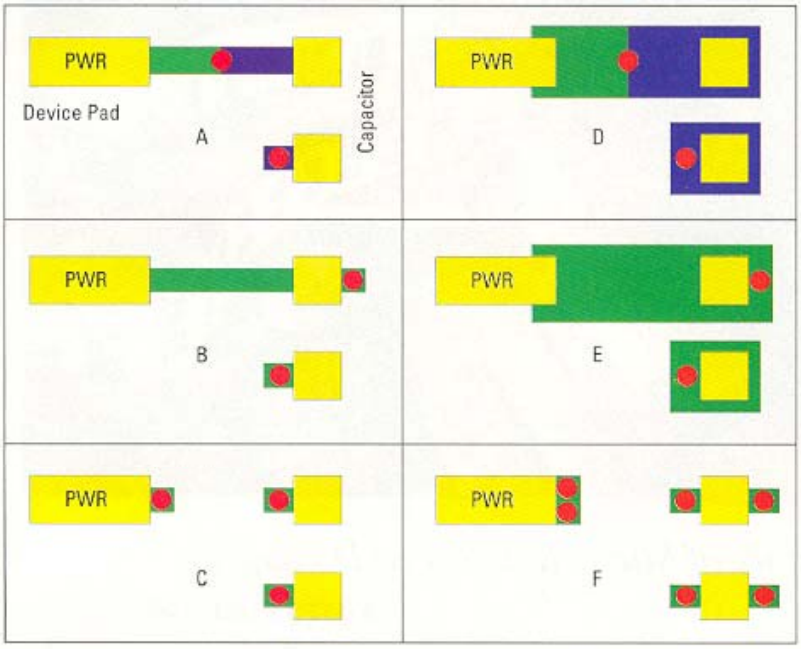
the inductance of the connection is the most important parameter of a local decoupling capacitor

none of the individual local decoupling capacitors are effective above a couple hundred megahertz, plane capacitance supplies most of the charge

none of the local decoupling capacitors are supplying significant charge in the first few nanoseconds of a transition.

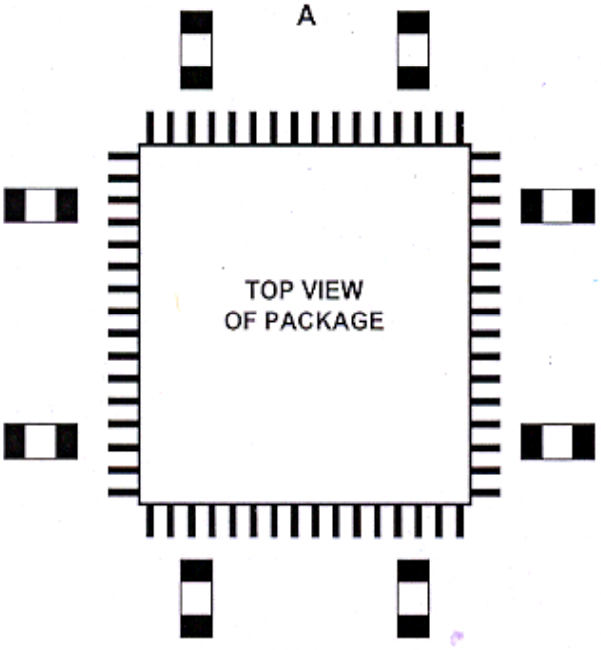
By Pass Capacitor Physical Layout



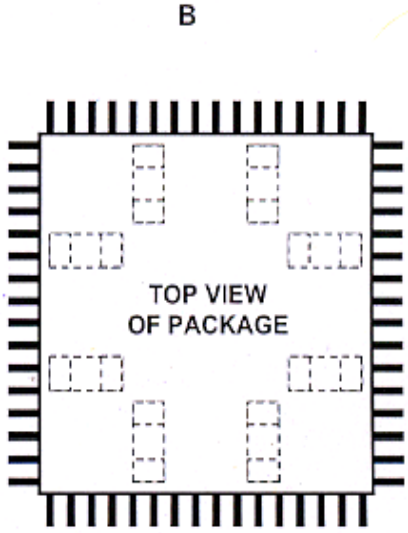


All are workable Solution dictated by Space available.
One via adds 1nH of Inductance.

Decoupling High Pin Count Chips

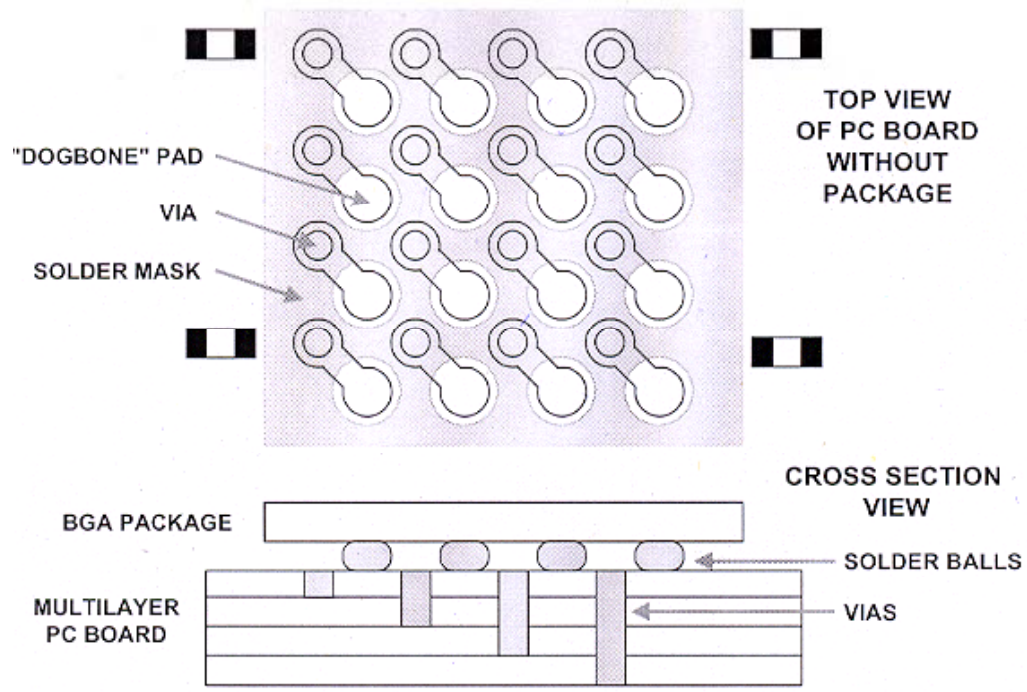


CAPACITORS ON TOP SIDE OF PC BOARD

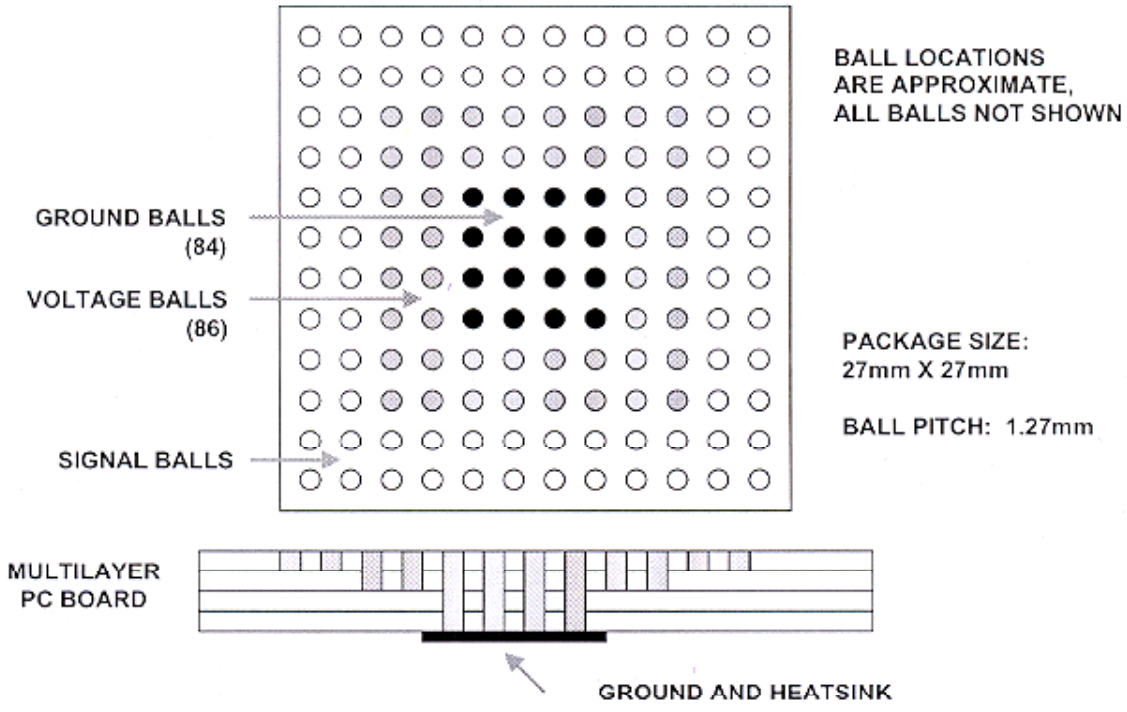


CAPACITORS ON BACK SIDE OF PC BOARD

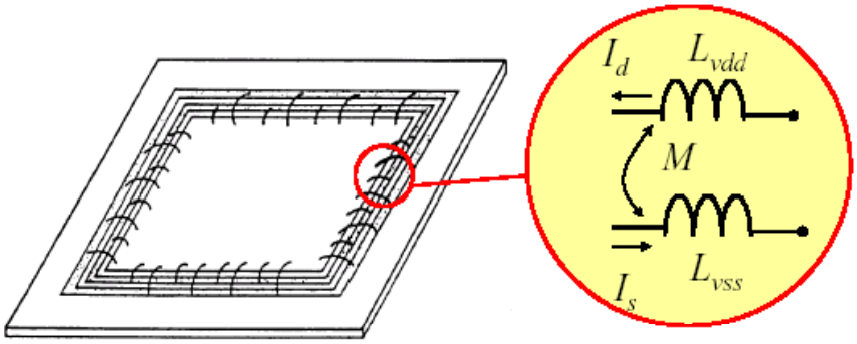
Decoupling BGA Packages

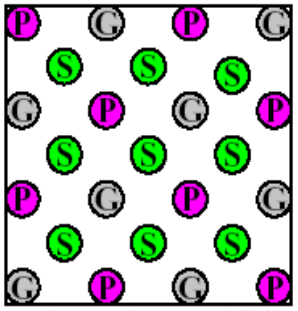


Decoupling BGA Packages



Low Inductance Packages





Area Array (C4)

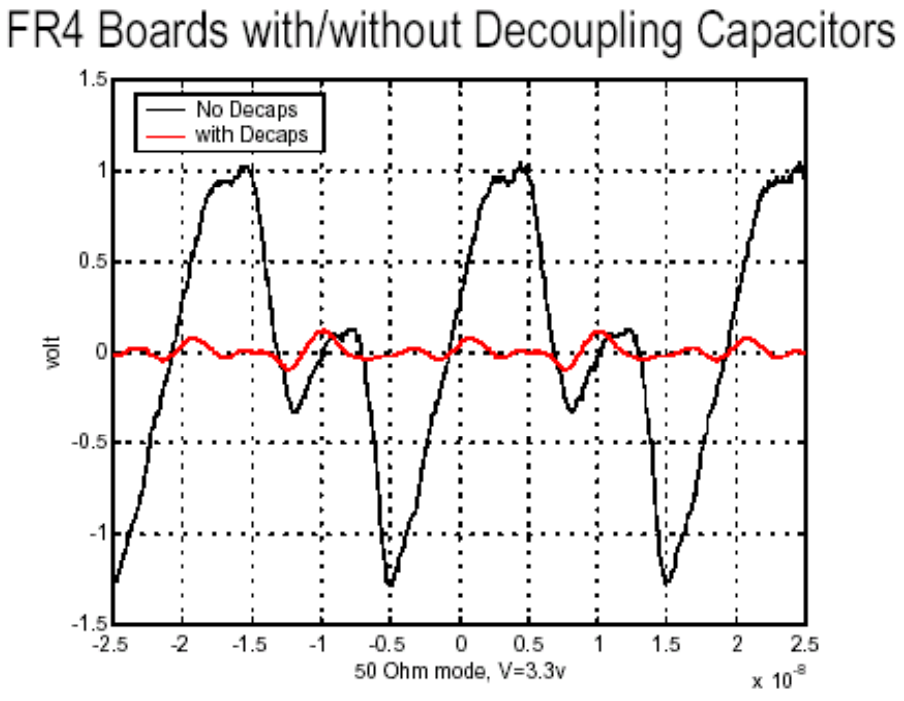
$$\Delta V_{dd} = L_{vdd}\frac{dI_d}{dt} - M\frac{dI_s}{dt}, \quad \Delta V_{ss} = L_{vss}\frac{dI_s}{dt} - M\frac{dI_d}{dt}$$

If $L_{vdd}=L_{vss}=L_p$, $I_s=I_d$, *Equivalent inductance (loop):* $L_{eq} = 2(L_p - M)$

Total Inductance: $\frac{1}{L_{total}} = \frac{1}{L_{eq1}} + \frac{1}{L_{eq2}} + \ldots$

Increase mutual coupling, increase # of power/ground pins, balance I_d and I_s locally

Typical Case: After Decoupling



Recommendation

- For Boards of up to 500MHz
  - For High Pin Count ICs
    - Use 10-22uf tantalum Cap with Every 20-50 PWR-GND Pins
    - Use 0.1-0.001uf Ceramic (X7R etc)Capacitor with Every 1-5 Pins for decoupling.
  - For Low Count General Purpose IC
    - One one 10-22uf tantalum Cap for every 50mA of Current.
    - Use 0.1-0.001uf Ceramic (X7R etc)Capacitor with Every 1-3 Pins for decoupling.

On-Chip Decoupling Capacitor

Hand Calculation

$$C_d = I\frac{\Delta t}{\Delta V} \qquad \text{(pessimistic)}$$

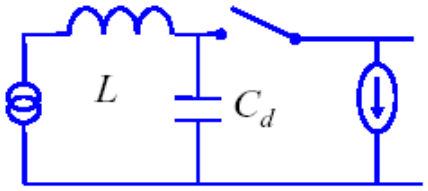
Δt: switching time, ΔV: allowed ripple voltage
t_{ck}: clock period, I_{avg}: time averaged current.
or

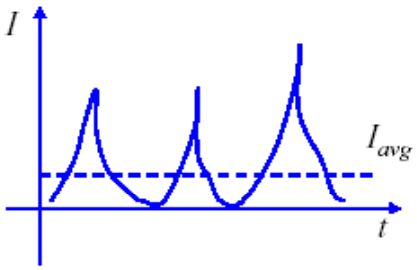
$$C_d > \frac{I_{avg}}{\Delta V}\left(k_i t_{ck} + \frac{LI_{avg}}{\Delta V}\right)$$

$$k_i = \max_t \frac{\left|\int_0^t (I - I_{avg})dt\right|}{I_{avg} t_{ck}}$$

Typically k_i=0.25~0.5

(k_i=1 for delta function, =0.25 for triangle wave, =0 for a DC current)

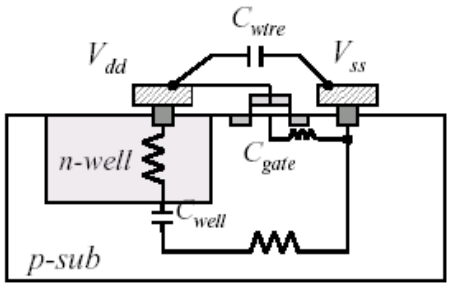




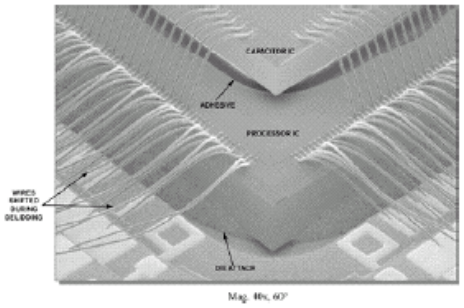
Industrial Example

IBM Power4:	~300nF of decoupling capacitors 4172 power and ground pins, 2208 signal pins (C4)
IBM Z900:	~250nF on-chip decoupling capacitors
Compaq EV6:	~320nF decoupling, occupy 15-20% chip area !

On-Module Capacitance

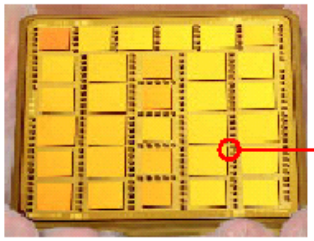


On-chip

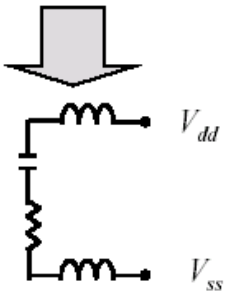


A capacitor chip is bonded to an DEC 21264 processor chip to provide power conditioning

"Near-chip"



IBM S390
MCM Module



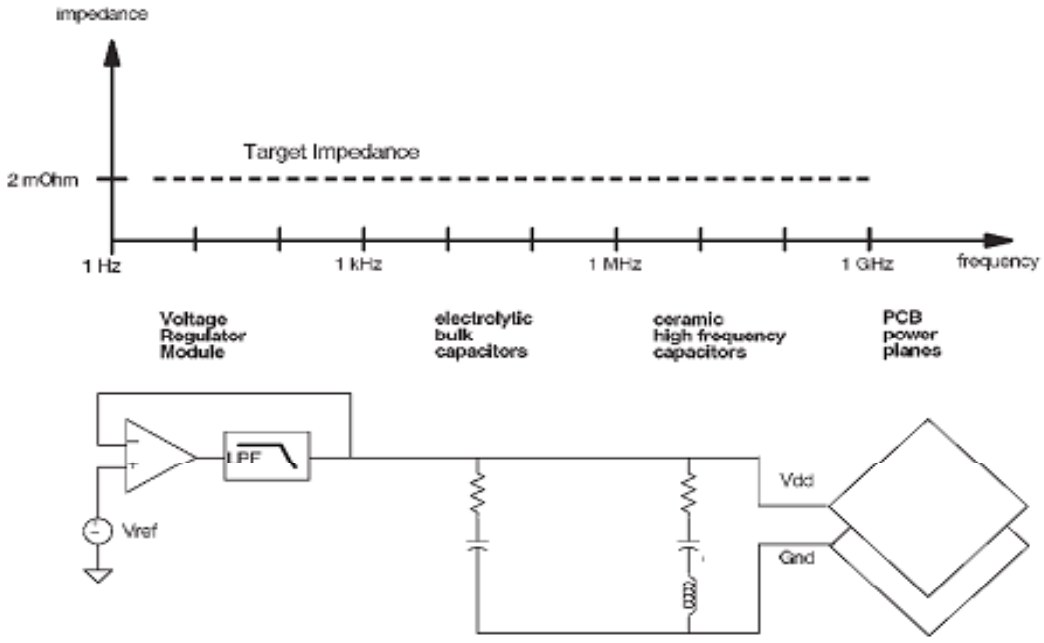
Off-chip (on-module)

Power and Ground Planes and Split planes

Power Planes

- Power-GND Plane pair is very High Quality capacitor with extremely Low ESR and ESL.
- Gives a lot of ease for Power and Ground Distribution
- Shields from EMI and enhances EMC

Power Distribution System



Each Component Supply the Current in Certain Frequency range and overall desired response is flat line.

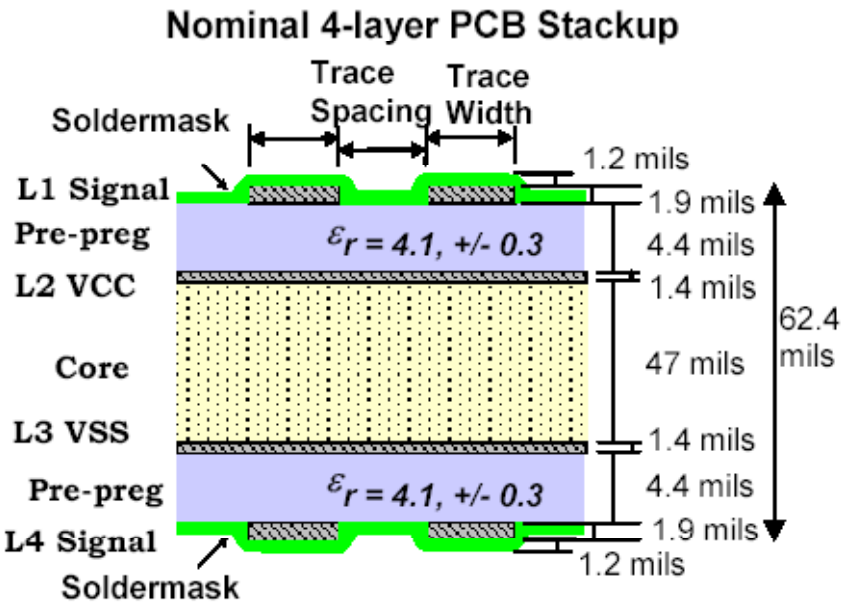
Popular Layer Stack-up

- No of Layers

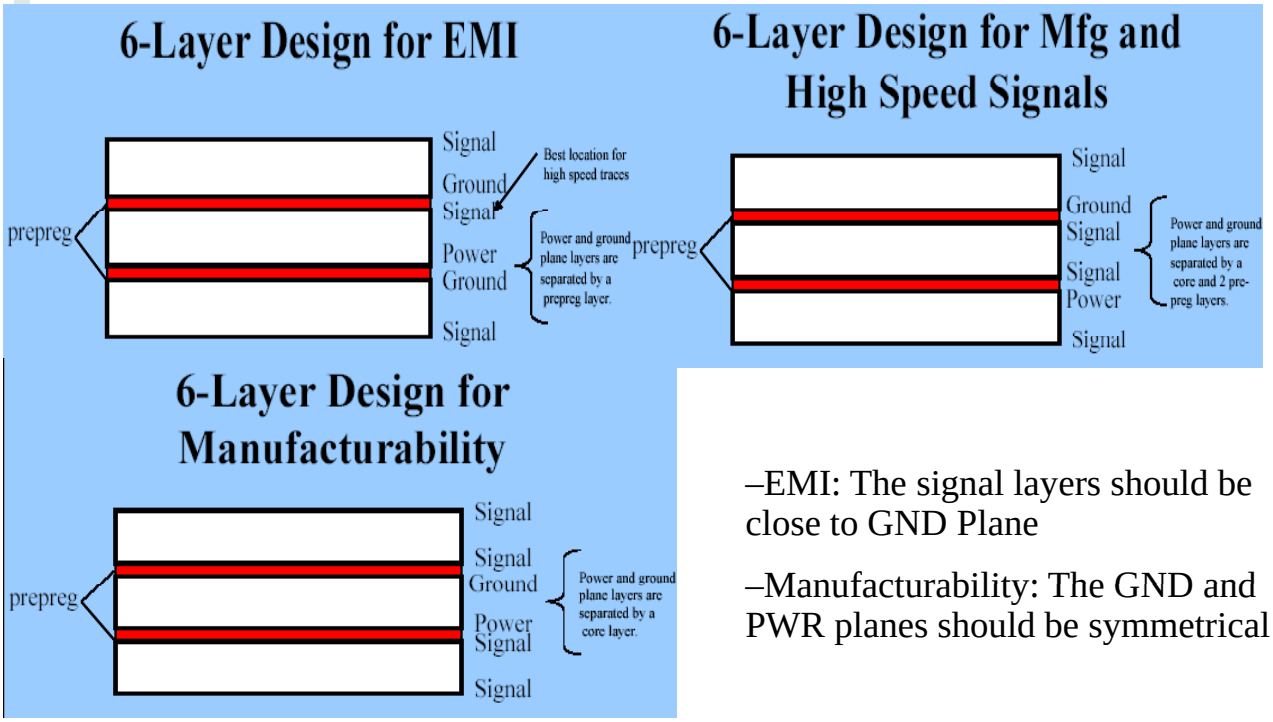
$$N_L = 4\log[D_n f_{CLK}]$$
$$D_n = Address\ or\ Data\ Bus$$

  - This is very Optimistic empirical Formula and good for frequencies > 50MHz
  - 66MHz, 32 Bit => 12 Layers, we can live with 8 or 10 layer if Component density is not too high.
- Typical Layer Stackup
  - 4 layers: layer 2,3 are power-ground
  - 6 layers: layer 2,5 are power-ground
  - 8 layers: Layer 2,7 are power-ground
  - 8 layers: Layer 2,4,5,7 are power-ground
  - 10 layer 2,8 are power-ground
  - 10 layer 2,4,7,9 are power-ground

Typical 4-Layer Stack



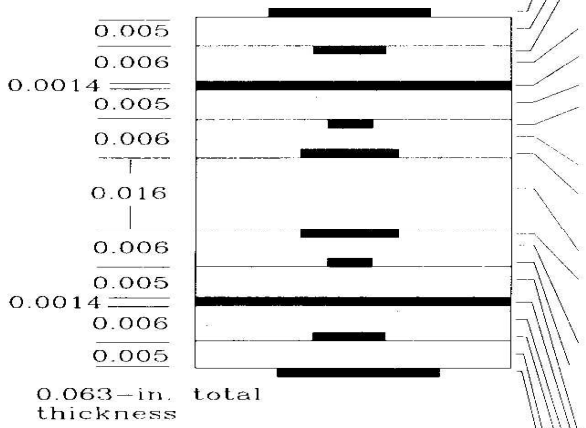
6 Layers: Comparison



–EMI: The signal layers should be close to GND Plane

–Manufacturability: The GND and PWR planes should be symmetrical

Typical 10-Layer Stack

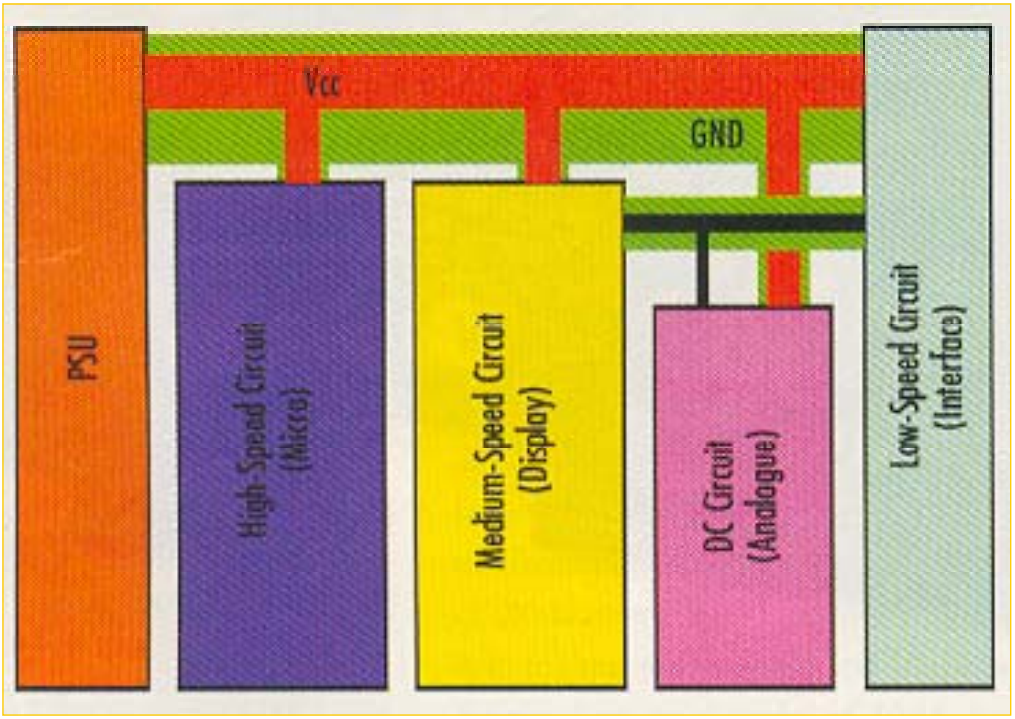


Layer 1: horizontal routing, 1–oz copper, 0.018–in. width, 0.050–in. pitch, 50 Ω (microstrip)
Core: 0.005–in. thick
Layer 2: vertical routing, 1 oz copper, 0.007–in. width, 0.025–in pitch, 50 Ω (embedded microstrip)
Prepreg: 0.006–in. thick
Layer 3: ground plane, 1–oz copper
Core: 0.005–in. thick
Layer 4: horizontal routing, 1–oz copper 0.006–in. width, 0.025–in. pitch, 50 Ω (offset stripline)
Prepreg: 0.006–in. thick
Layer 5: vertical routing, 1 oz copper, 0.011–in. width, 0.050 in. pitch, 50 Ω (offset stripline)
Core: 0.016–in. thick
Layer 6: horizontal routing, 1–oz copper, 0.011–in. width, 0.050–in. pitch, 50 Ω (offset stripline)
Prepreg: 0.006–in. thick
Layer 7: vertical routing, 1–oz copper, 0.006–in. width, 0.025–in pitch, 50 Ω (offset stripline)
Core: 0.005–in. thick
Layer 8: 5 V power plane, 1–oz copper
Prepreg: 0.006–in. thick
Layer 9: horizontal routing, 1–oz copper, 0.007–in. width, 0.025–in. pitch, 50 Ω (embedded microstrip)
Core: 0.005–in. thick
Layer 10: vertical routing, 1–oz copper, 0.018 in. width, 0.050–in. pitch, 50 Ω (microstrip)

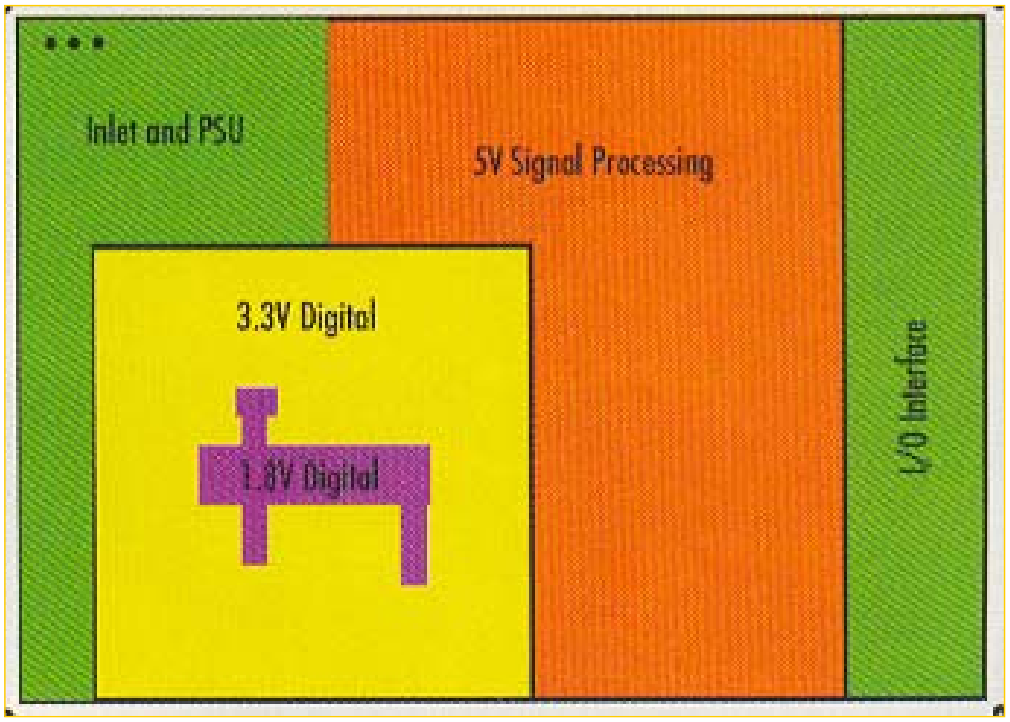
Comments:
(1) Same trace sizes and tolerance issues as in Figure 5.25, but adds four more routing layers.
(2) Layers 2 and 8 are embedded in dielectric and thus will have lower impedance than that calculated using a simple microstrip assumption.
(3) Crosstalk between layers 4 and 6 (or 5 and 7) is determined by the ratio of separation to ground plane height. Minimum separation is 0.022 in., geometric average height is 0.007 in., ratio 0.022/0.007 is 3.
(4) Routing layers 2 and 9 tend to sink into the prepreg and thus need 0.006–in. prepreg to achieve 0.005–in. nominal height above ground.

Figure 5.26 Ten-layer stack.

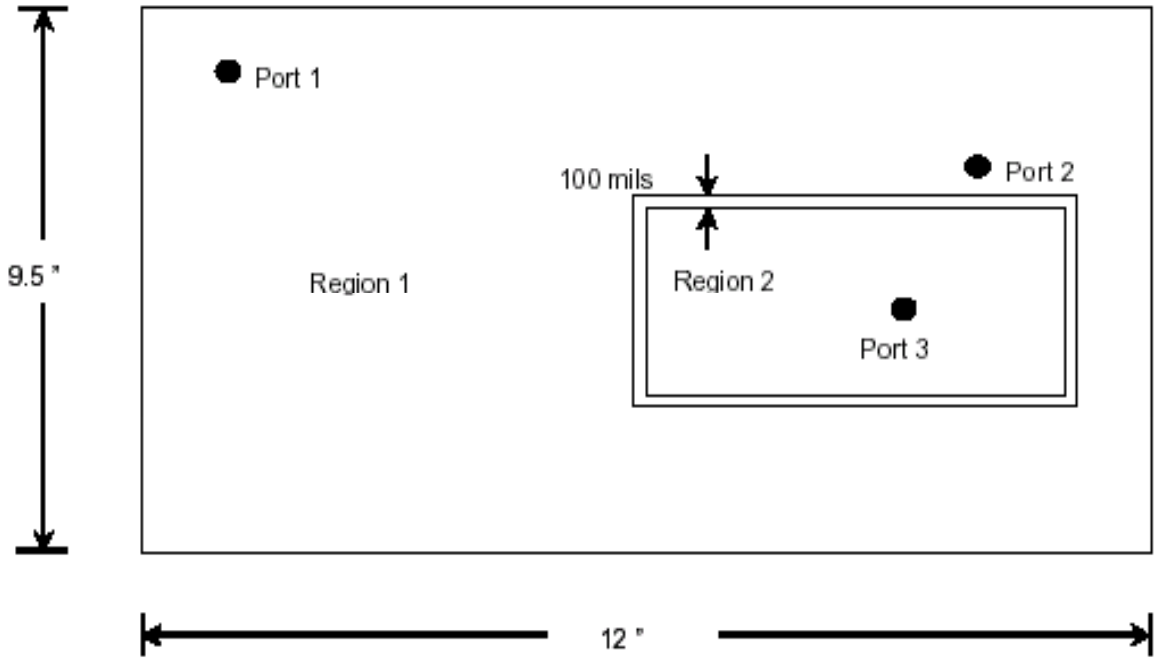
Idealized Circuit Segmentation



Corresponding Split GND-PWR Planes

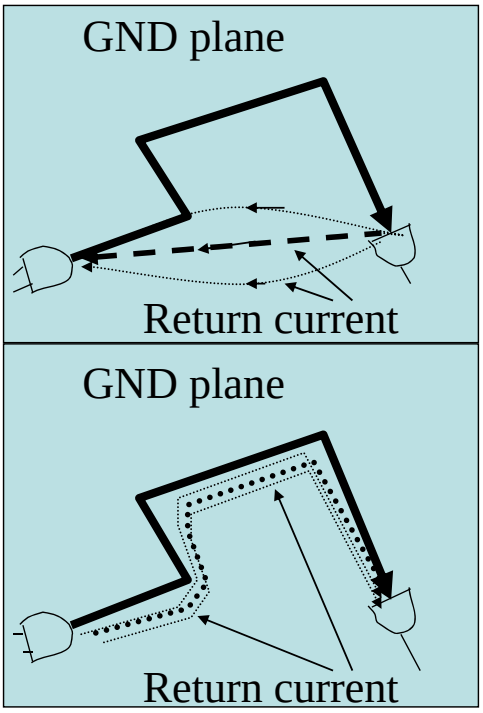


Split GND-PWR Planes: 100 Mils, No Hole



GND Planes

- Functions of ground planes
  - Provide stable reference voltages
  - Distribute power to devices
  - Control cross-talk between signals
- At high speed , the inductance of its return path is far more important than its resistance.

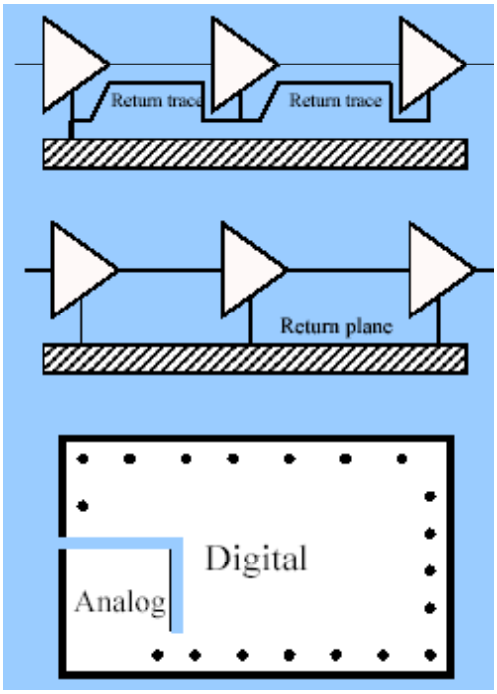


GND Planes are Mandatory

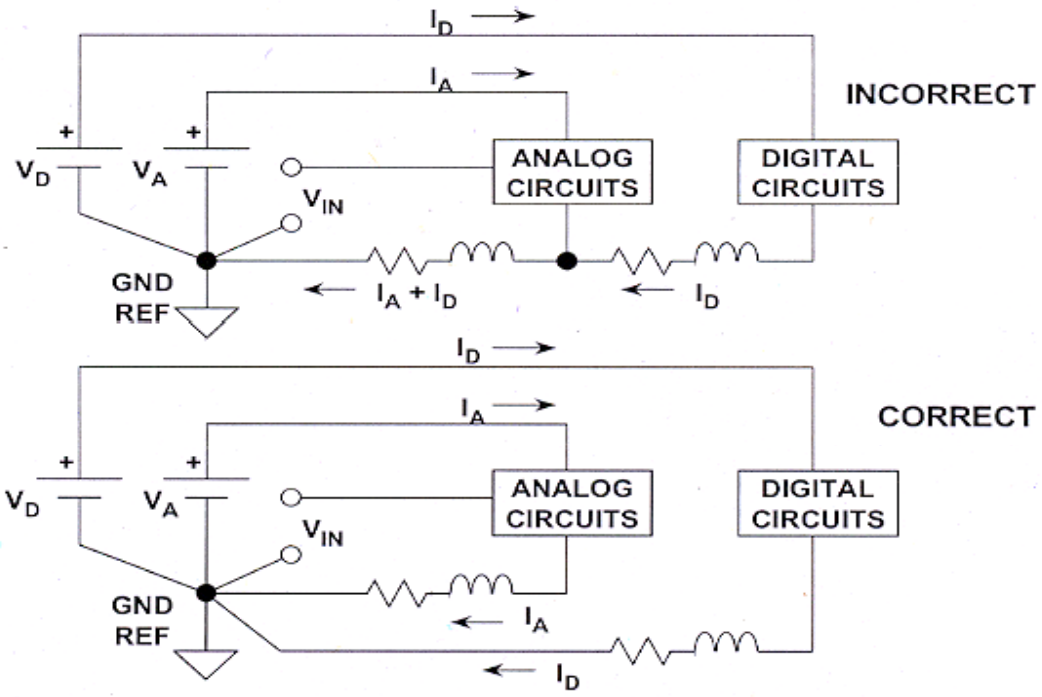
- Use Large Area Ground (and Power) Planes for Low Impedance Current Return Paths (Must Use at Least a Double-Sided Board!)
- Double-Sided Boards:
  - Avoid High-Density Interconnection Crossovers and Vias Which Reduce Ground Plane Area
  - Keep > 75% Board Area on One Side for Ground Plane
- Multilayer Boards: Mandatory for Dense Systems
  - Dedicate at Least One Layer for the Ground Plane
  - Dedicate at Least One Layer for the Power Plane
- Use at Least 30% to 40% of PCB Connector Pins for Ground
- Continue the Ground Plane on the Backplane Motherboard to Power Supply Return

Grounding Topologies

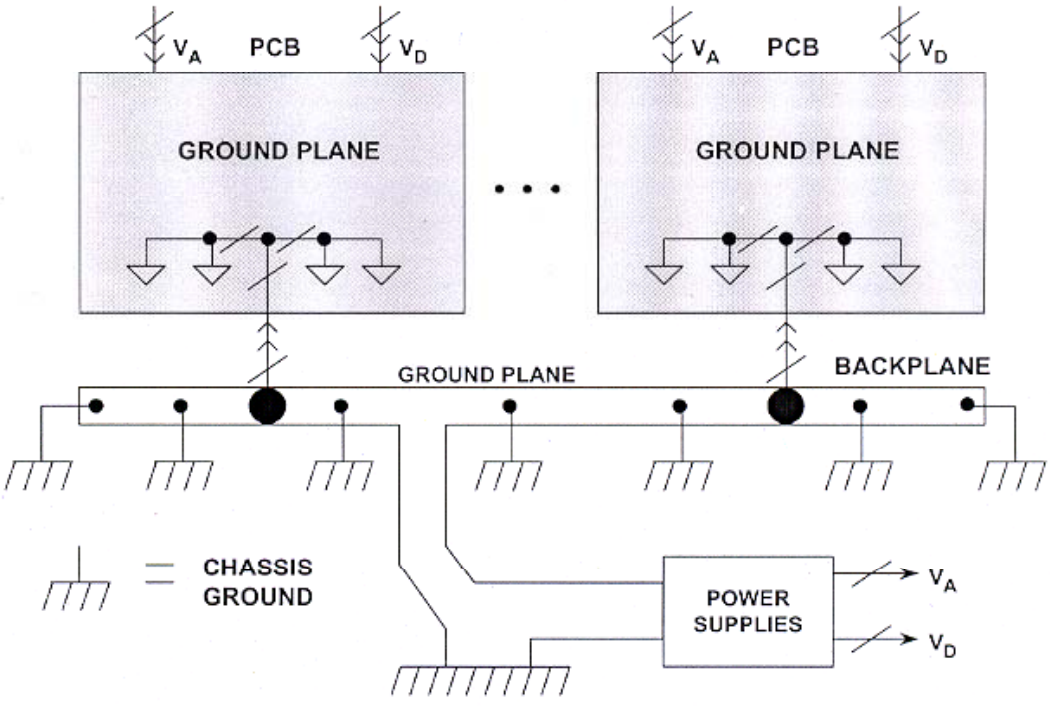
- Single Point
- Multipoint
- Hybrid



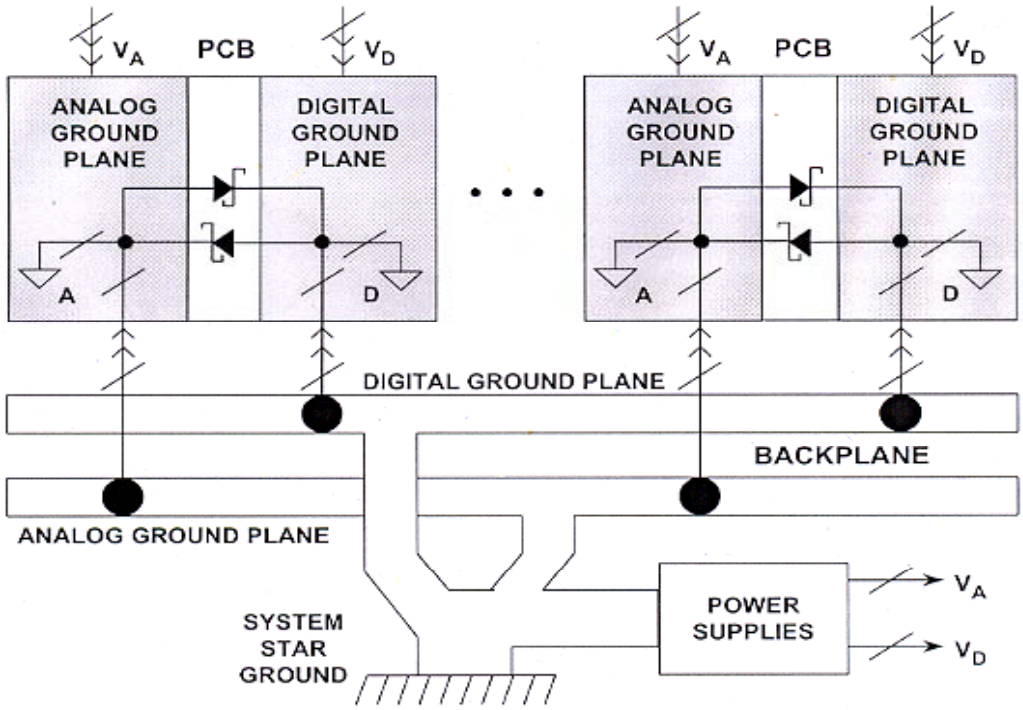
Grounding Techniques: One-Point GND



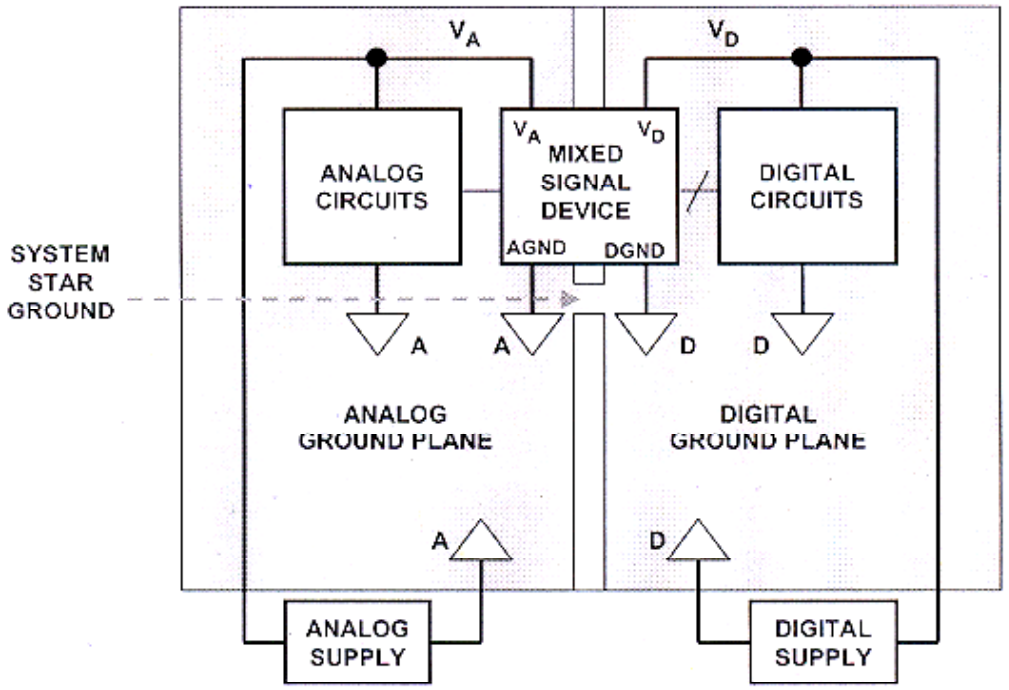
Grounding Techniques: Back Plane



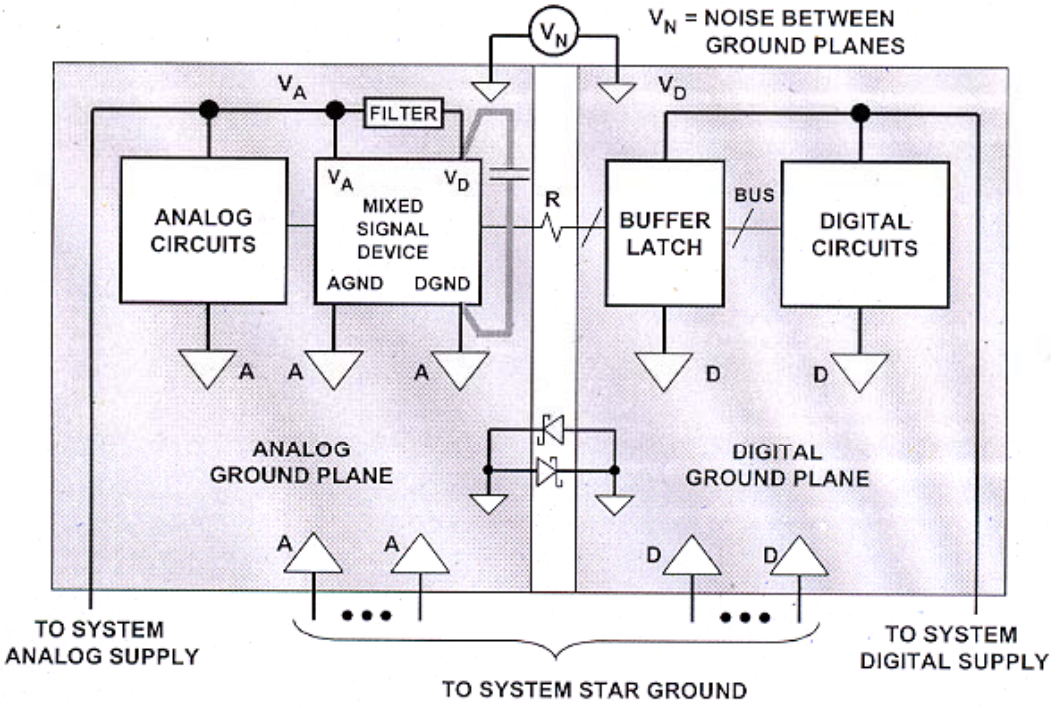
Separation of Digital and Analog GND



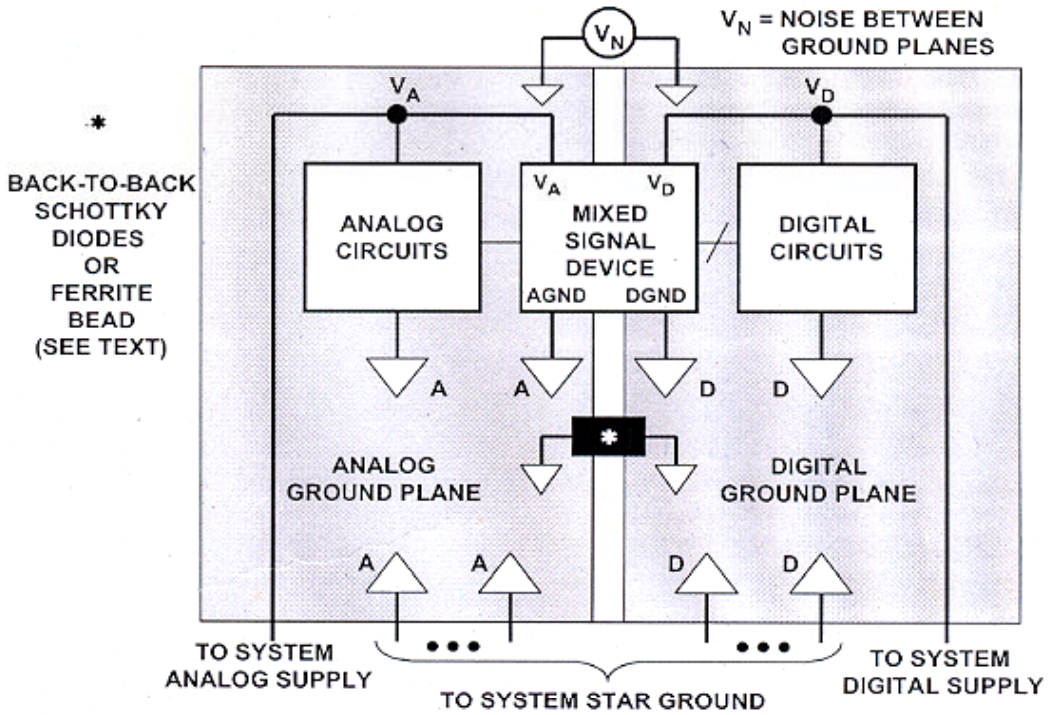
Mixed Signal IC Grounding: Same Board



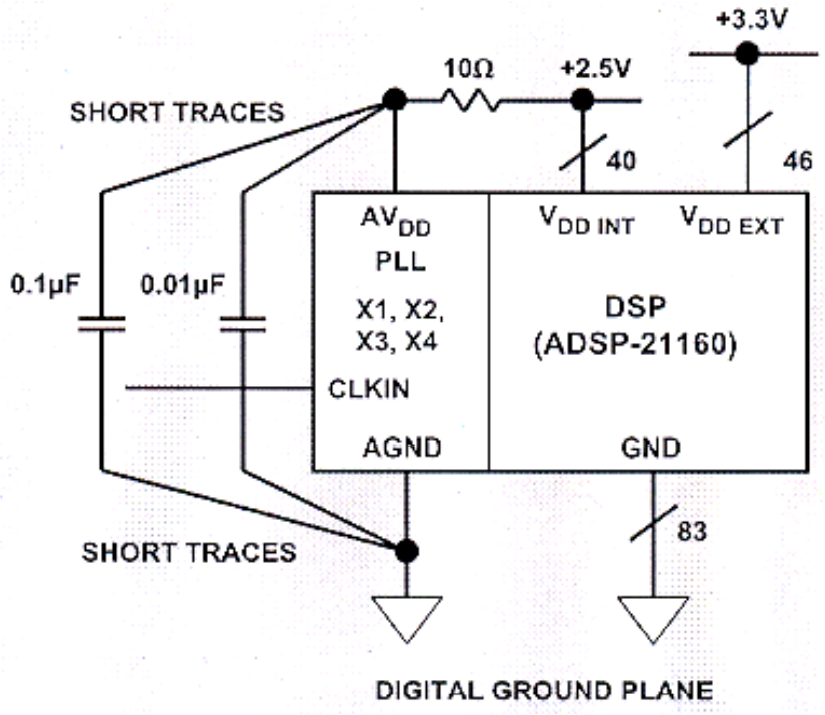
Mixed Signal IC Grounding-1: Different Board



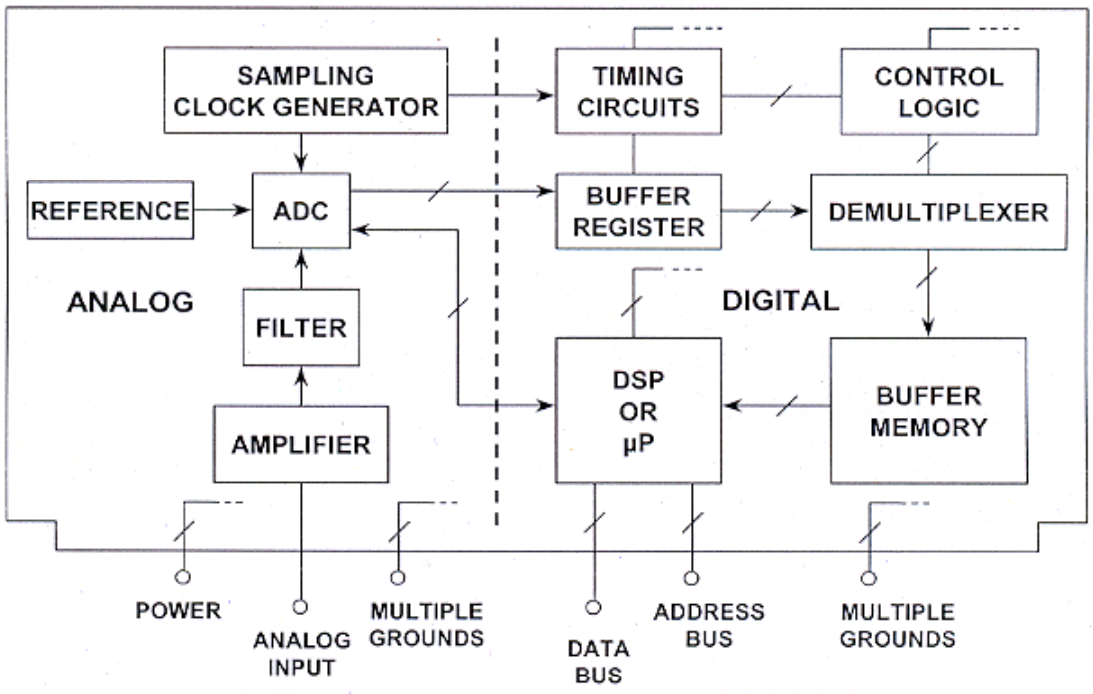
Mixed Signal IC Grounding-2: Different Board



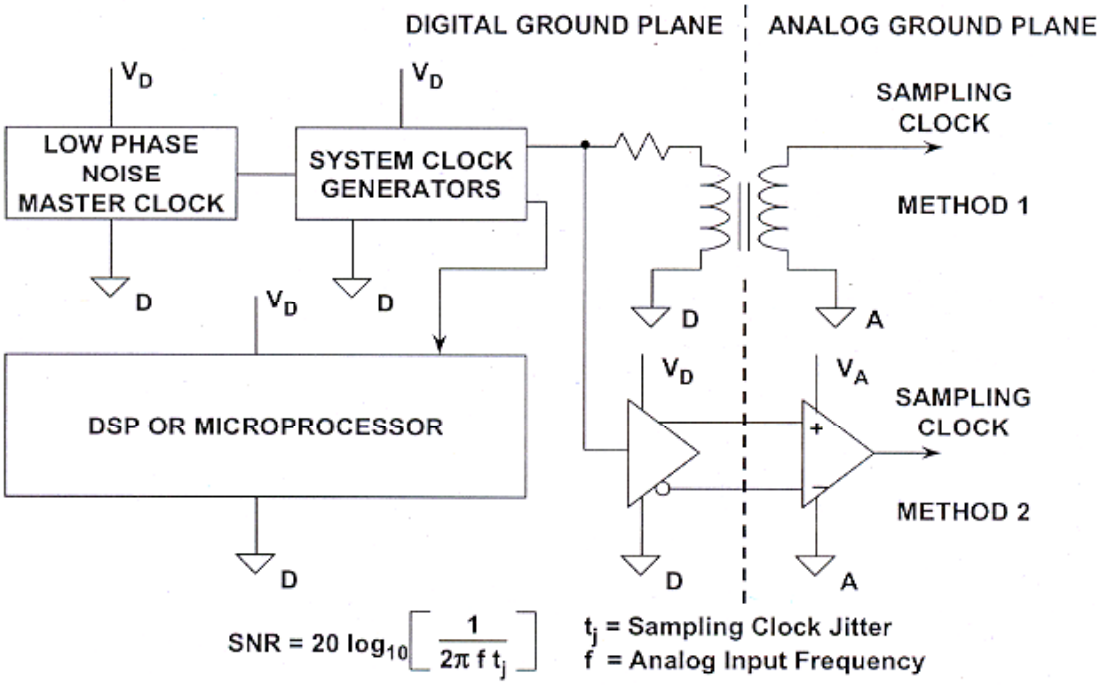
FPGA or DSP with Internal PLL



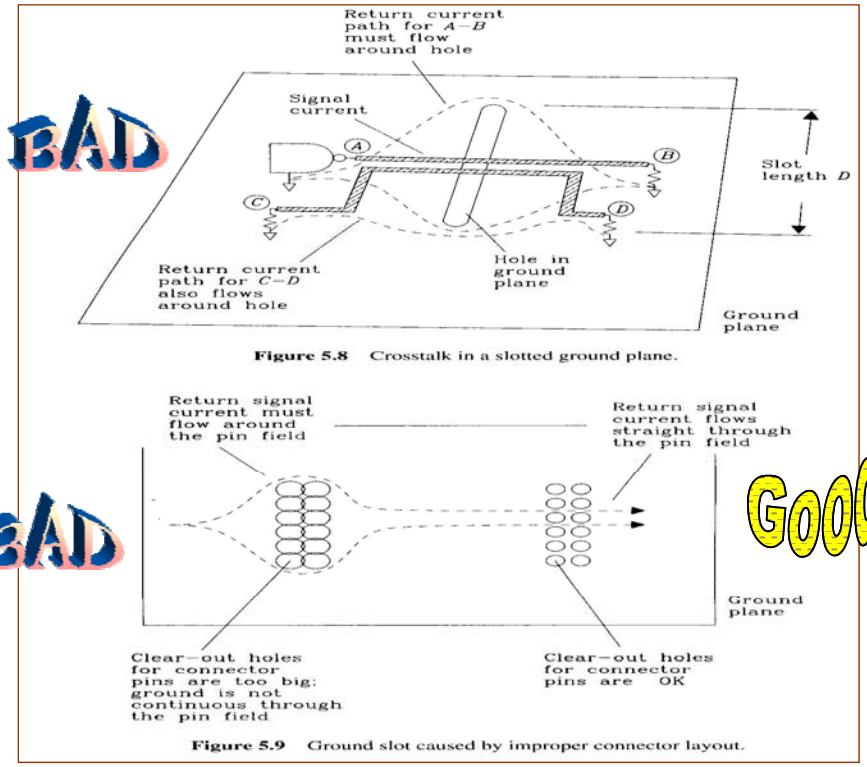
Mixed Signal Board Portioning



CLK from DGND to AGND



Slots in GND Planes



Summary

- There is no single grounding method which is guaranteed to work 100% of the time!
- Different methods may or may not give the same levels of performance.
- At least one layer on each PC board MUST be dedicated to ground plane!
- Do initial layout with split analog and digital ground planes.
- Provide pads and vias on each PC board for back-to-back Schottky diodes and optional ferrite beads to connect the two planes.
- Provide "jumpers" so that DGND pins of mixed-signal devices can be connected to AGND pins (analog ground plane) or to digital ground plane. (AGND of PLLs in DSPs should be connected to digital ground plane).
- Provide pads and vias for "jumpers" so that analog and digital ground planes can be joined together at several points on each PC board.
- Follow recommendations on mixed signal device data sheet.

Wakeup Please lets have Some Food....