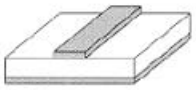
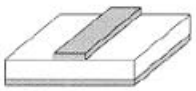


SI Tools, DFM, Thermal Analysis and Rules of Thumb

Rashad.M.Ramzan, Ph.D

FAST-NU, Islamabad



Summary

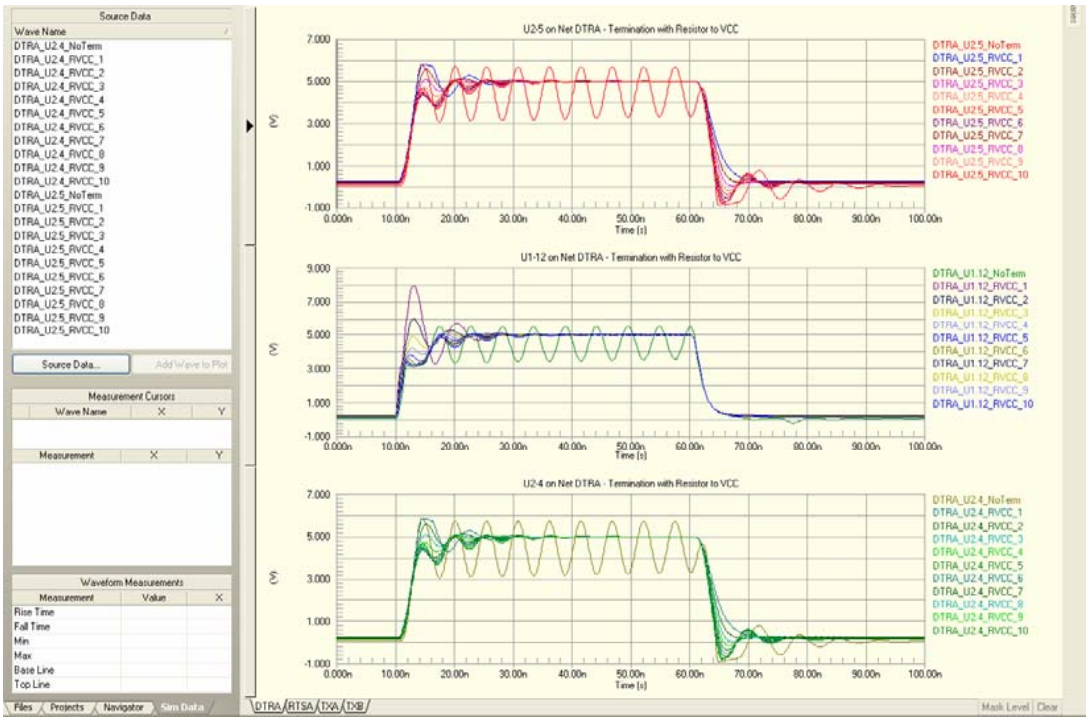
- Signal Integrity Tools
  - Simulation Tools: … a lot of Manufacturers
  - TDR (Time Domain Reflectometry)
- DFM (Design For Manufacturability)
- Thermal Analysis
- Rule of Thumb, Every PCB Designer should remember

Altium Signal Integrity

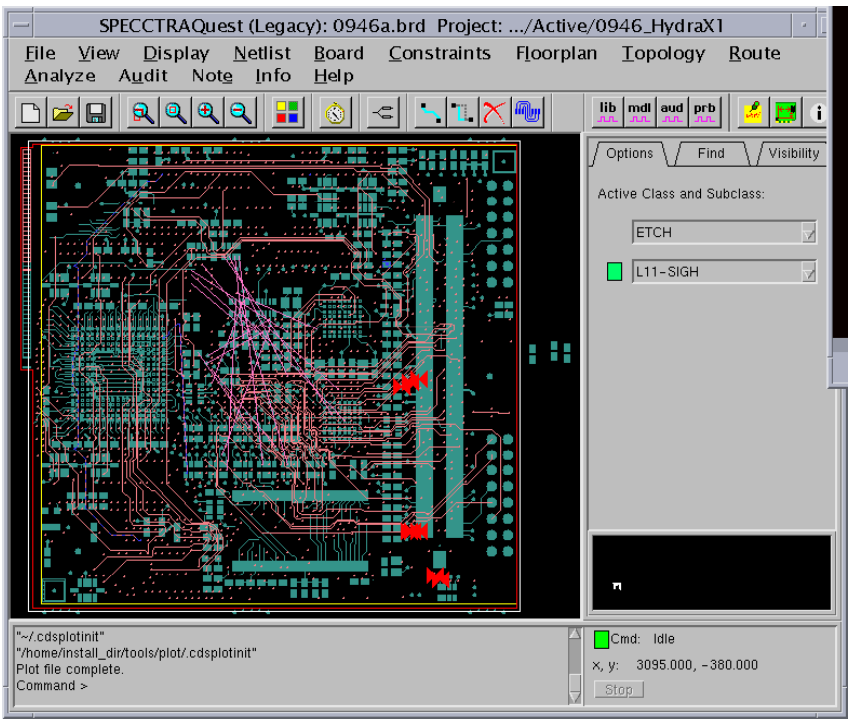
- Perform signal integrity analysis at the
  - capture stage and
  - during board layout.
- How its Helpful?
  - Identify potential problem areas before moving to PCB layout.
- Capabilities
  - Impedance determination
  - Signal reflection and
  - Crosstalk analysis
- Signal integrity screening is built into the Altium Designer design rules system, allowing to check for potential signal integrity violations as part of the normal board DRC process.

We will discuss more details in LAB sessions

Altium Signal Integrity



SpecctraQuest (SI Tool)



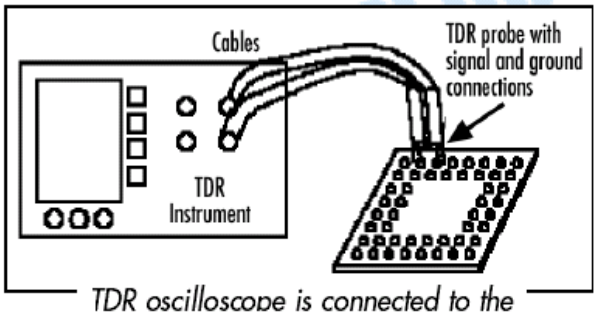
- **Impedance**
- **Reflection**
- **Crosstalk**
- **EMI**
- **EMC**
- **Thermal Profiling**
- **Statistical Analysis**

Based upon
- **IBIS Models**
- **SPICE Models**

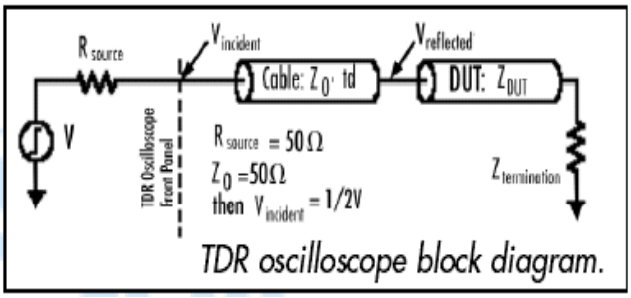
TDR(Time Domain Reflectometry)

- Time Domain Reflectometry
  - Initially Used for finding cable faults, Now combined with Signal Integrity Analysis Tools, its used for detecting faults in Boards, Packages, Socket and Cable interconnects at Giga Bit rates.
  - TDR oscilloscope is very popular for SI and Interconnect Characteristic. Its very visual and intuitive technology , its wave forms can be easily correlated to Physical structure of Interconnect.

TDR Oscilloscope



TDR oscilloscope is connected to the device under test via cables, probes and fixtures.



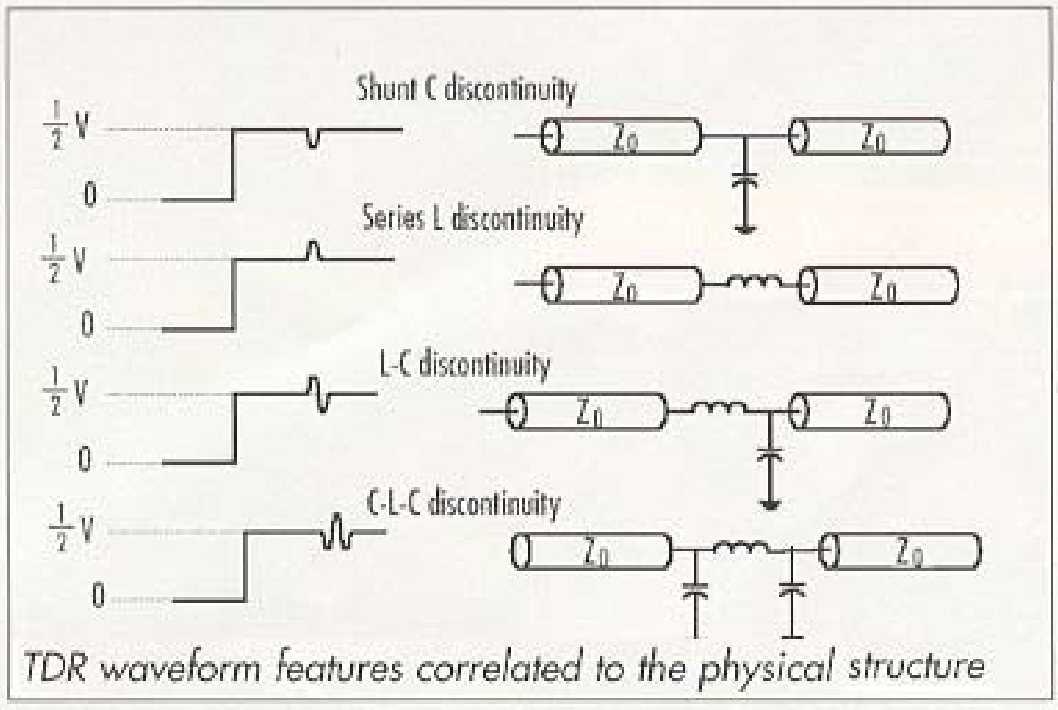
TDR oscilloscope block diagram.

- TDR instruments are very wideband equivalent sampling of 18-20GHz.
- Principle:
  - Transmission Line Theory

$$Z_{DUT} = Z_o \frac{1+\rho}{1-\rho}$$

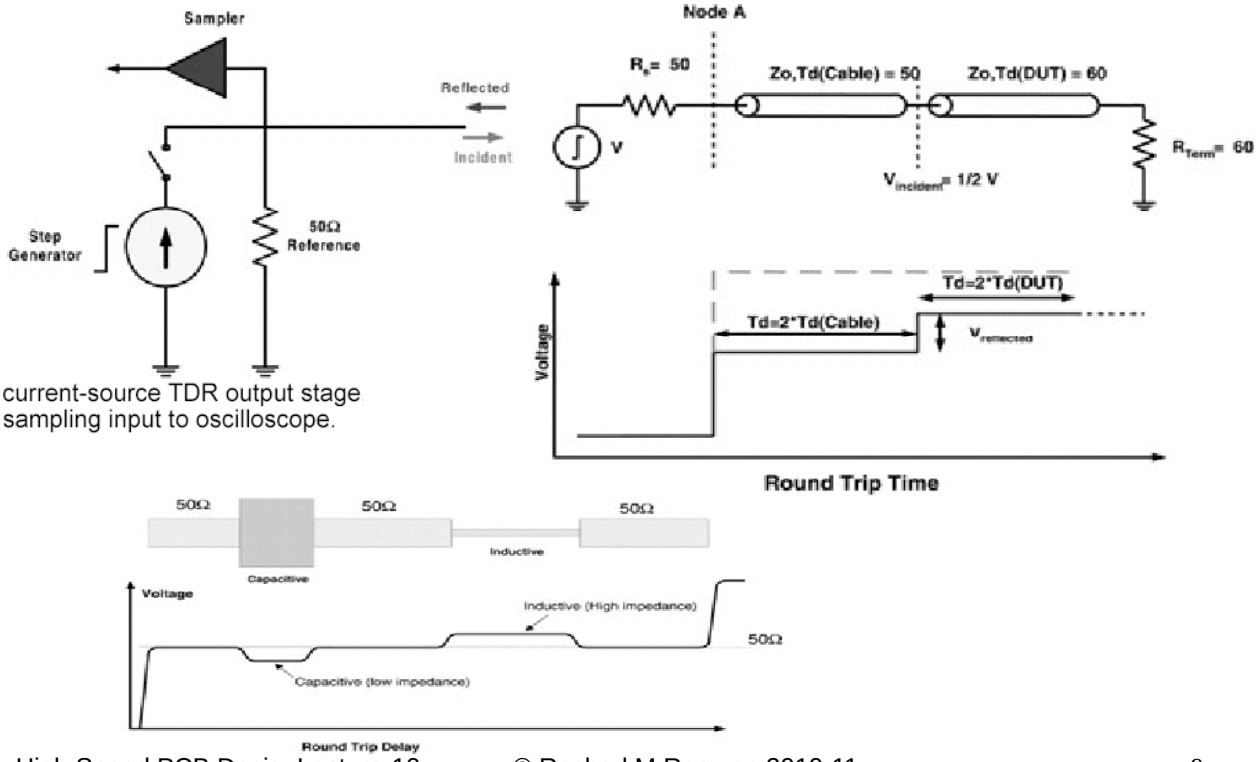
$$\rho = \frac{V_{reflected}}{V_{incident}} = \frac{Z_{DUT} - Z_o}{Z_{DUT} + Z_o}$$

TDR Waveforms

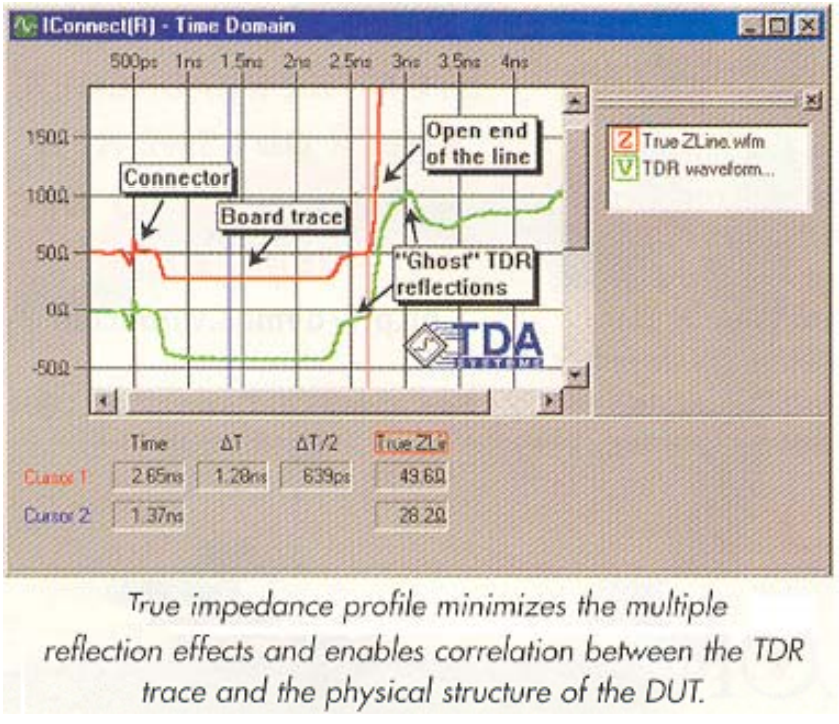


TDR waveform features correlated to the physical structure

TDR Waveforms



TDR Waveforms



True impedance profile minimizes the multiple reflection effects and enables correlation between the TDR trace and the physical structure of the DUT.

Impedance deconvolution algorithms for separating the responses at different time.

The Probe has its own impedance that generates the Ghost images

Measurement of Input Packages and Die capacitances

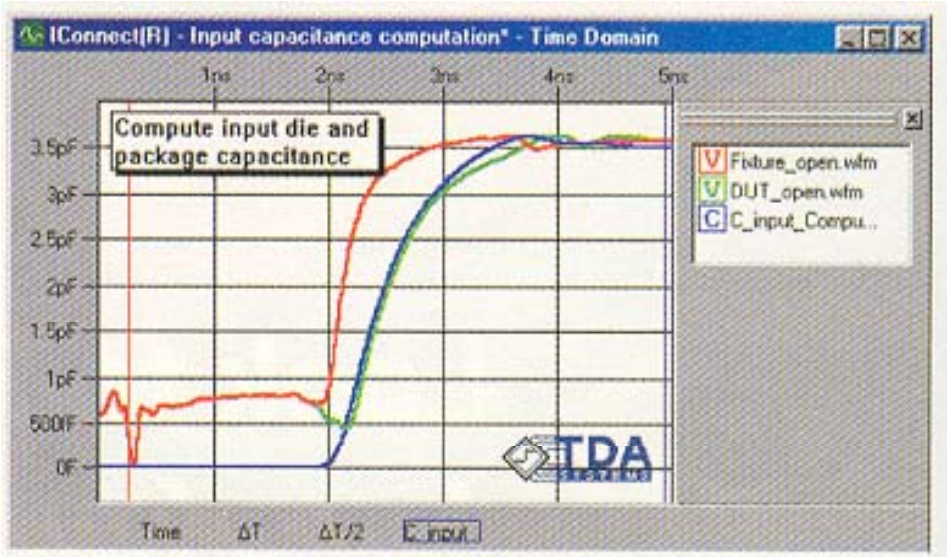
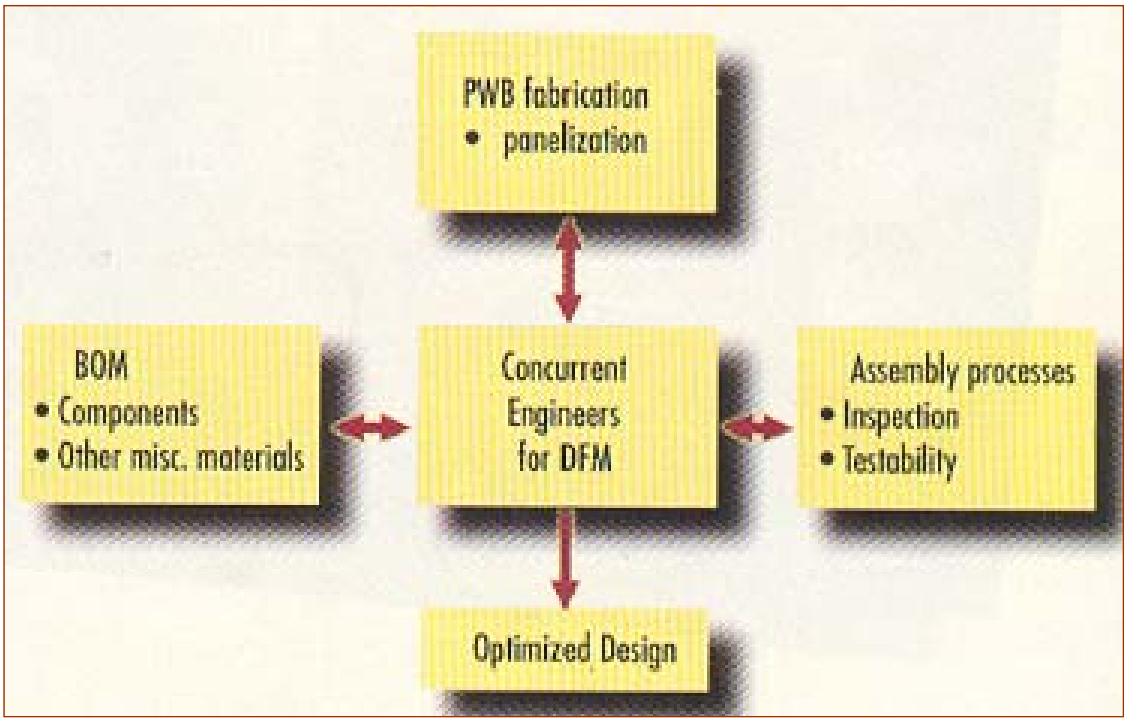


Figure 5 - *Compute input die and package capacitance from the TDR analysis. The capacitive value here is estimated to be 3.5 pF.*

Typical Design Consideration

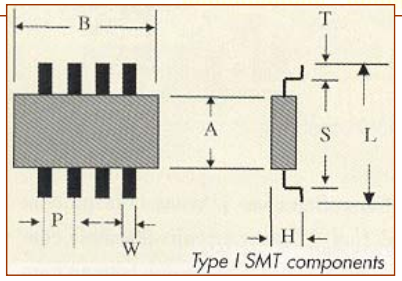


PCB Cost Factors

1. Advance technologies
   - Laser Drilling
2. Increasing PCB Size (More Material Utilization)
3. Increasing no of Layers
4. Reducing Line width and Spacing
5. Increasing Drilled Hole Count
6. Reducing Drill Hole Diameters
7. Adding Buried Cap and resistors
8. Adding Blind Vias
9. Gold Plating Requirements
10. Improved HF Material (>> FR4)
11. Controlled Impedance
12. Via Plugging

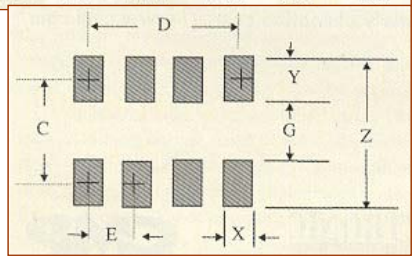
Land Pattern Generation

Comp. Identifier	JEDEC Number	L mm/in min	L mm/in max	S mm/in min	S mm/in max	W mm/in min	W mm/in max	T mm/in min	T mm/in max	A mm/in min	A mm/in max	B mm/in Min	B mm/in max
SO8	MS-012	5.80	6.20	3.26	4.55	0.33	0.51	0.40	1.27	3.80	4.00	4.80	5.00
	AA	0.228	0.244	0.128	0.179	0.013	0.020	0.016	0.050	0.150	0.157	0.189	0.197
SO14	MS-012	5.80	6.20	3.26	4.55	0.33	0.51	0.40	1.27	3.80	4.00	8.55	8.75
	AB	0.228	0.244	0.128	0.179	0.013	0.020	0.016	0.050	0.150	0.157	0.337	0.344
SO16	MS-012	5.80	6.20	3.26	4.55	0.33	0.51	0.40	1.27	3.80	4.00	9.80	10.00
	AC	0.228	0.244	0.128	0.179	0.013	0.020	0.016	0.050	0.150	0.157	0.386	0.394



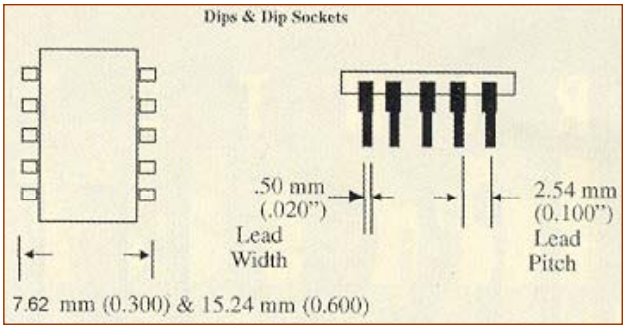
Type I SMT components

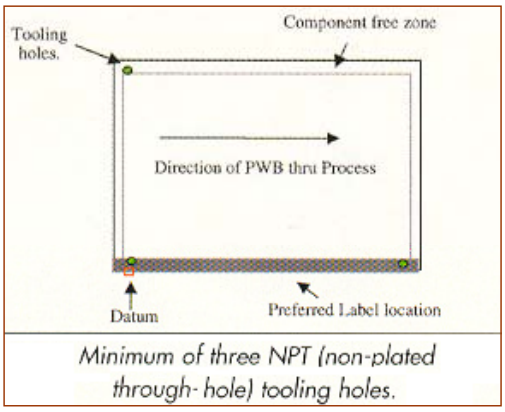
Component Identifier	Ref. IPC RLP No.	Z mm/in	G mm/in	X mm/in	Y mm/in ref	C mm/in ref	D mm/in ref	E mm in ref
SO8	300AR	6.60	2.86	0.65	1.87	4.73	3.81	1.27
		0.260	0.113	0.026	0.074	0.186	0.15	0.050
SO14	302AR	6.60	2.86	0.65	1.87	4.73	7.62	1.27
		0.260	0.113	0.026	0.074	0.186	0.30	0.050
SO16	304AR	6.60	2.86	0.65	1.87	4.73	8.89	1.27
		0.260	0.113	0.026	0.074	0.186	0.35	0.050



THD and Tooling Holes

- The finished hole size should be 7 mil greater then max pin width or diameter.
- Tooling Holes





Minimum of three NPT (non-plated through-hole) tooling holes.

Component Spacing

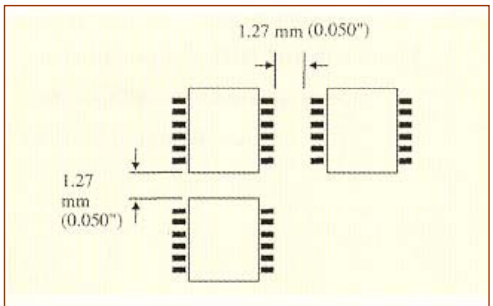


Figure 8 – SMD to SMD. Note: Spacing relationship from SOIC to SOIC

•Beside Component to component spacing Component to Via spacing Should also be considered to avoid solder bridging and secondary reflow.

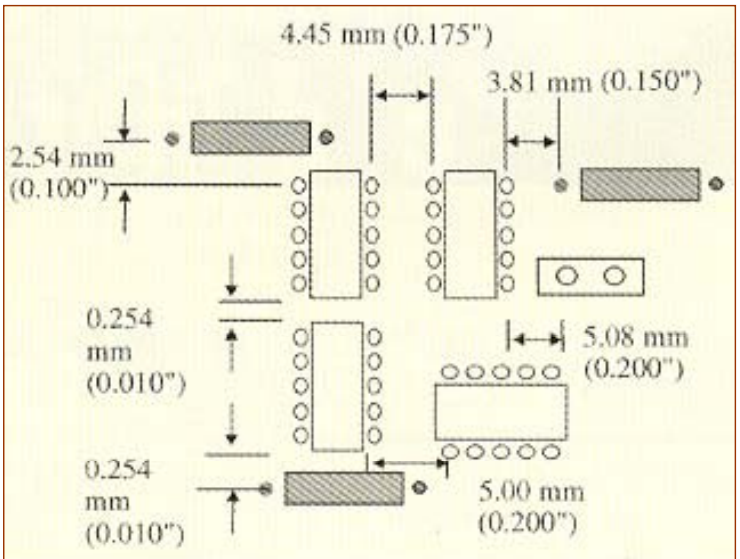
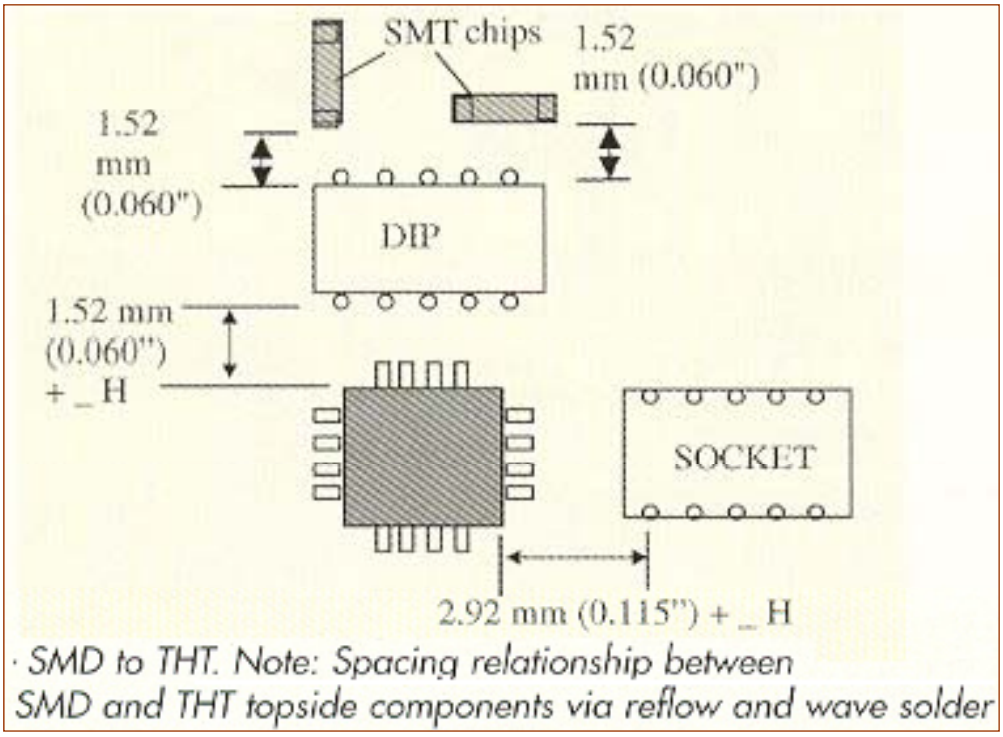


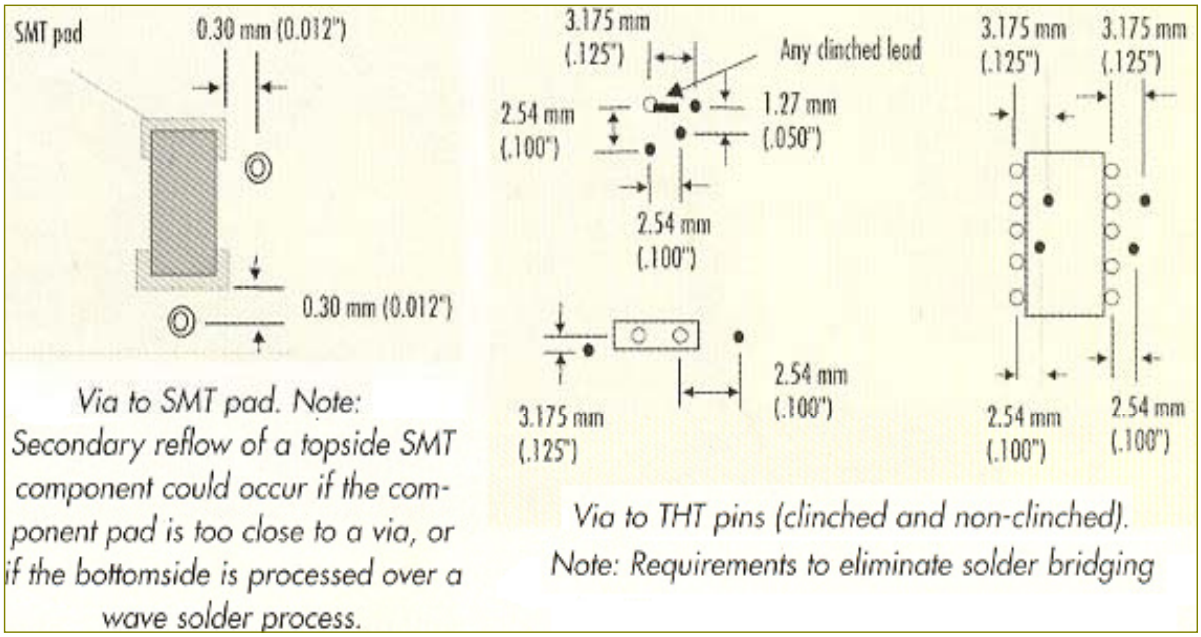
Figure 7 – Through-hole to through-hole. Note: Spacing relationship from DIP to DIP, DIP to AXIAL, and DIP to RADIAL, etc.

Component Spacing



· SMD to THT. Note: Spacing relationship between SMD and THT topside components via reflow and wave solder

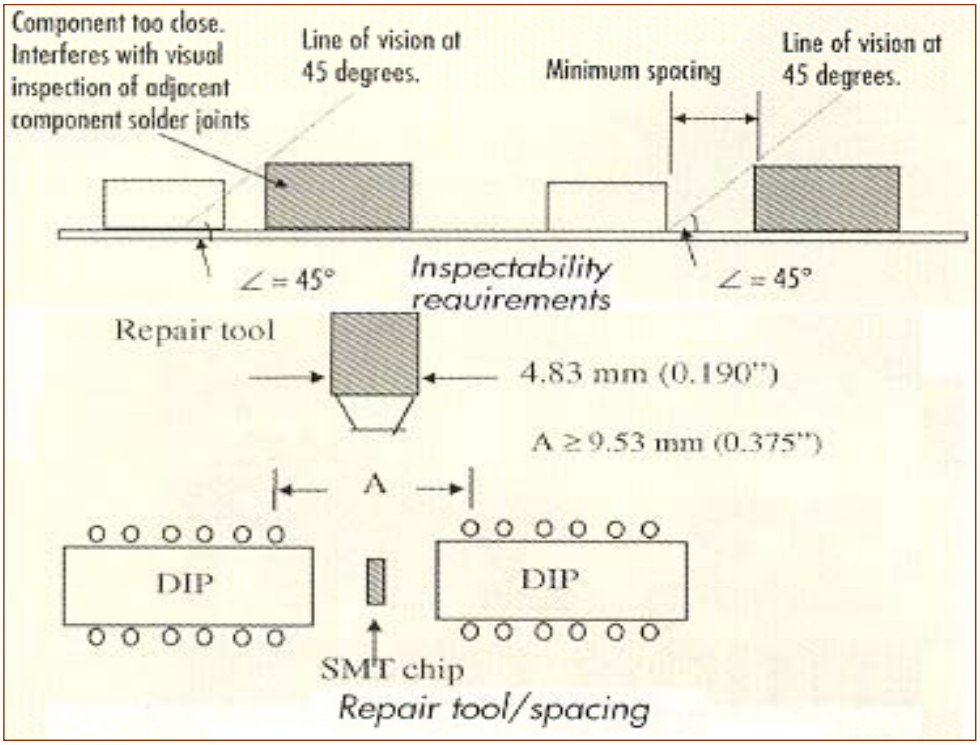
Component Spacing to PCB via Holes



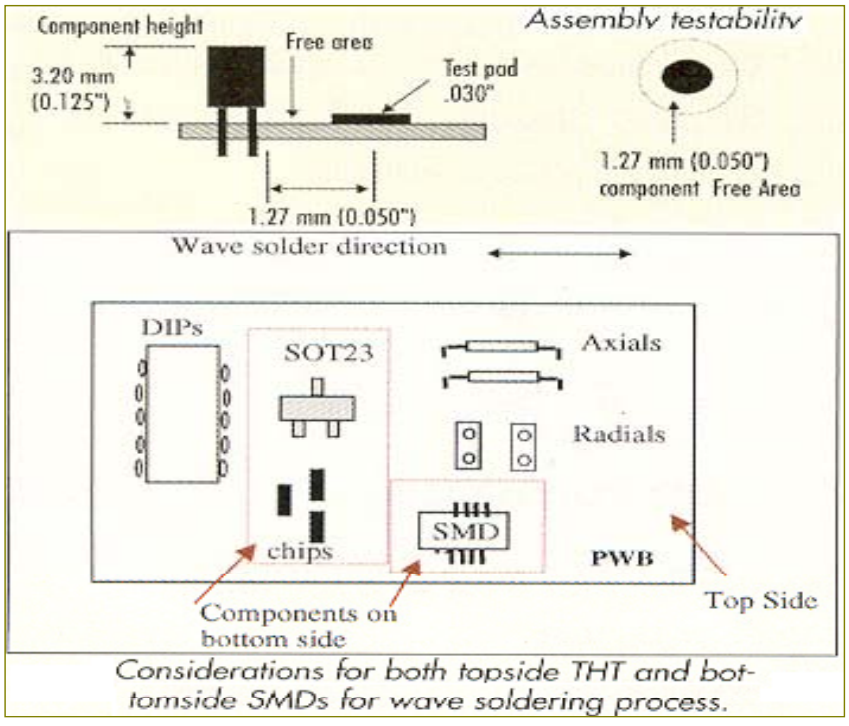
Via to SMT pad. Note: Secondary reflow of a topside SMT component could occur if the component pad is too close to a via, or if the bottomside is processed over a wave solder process.

Via to THT pins (clinched and non-clinched). Note: Requirements to eliminate solder bridging

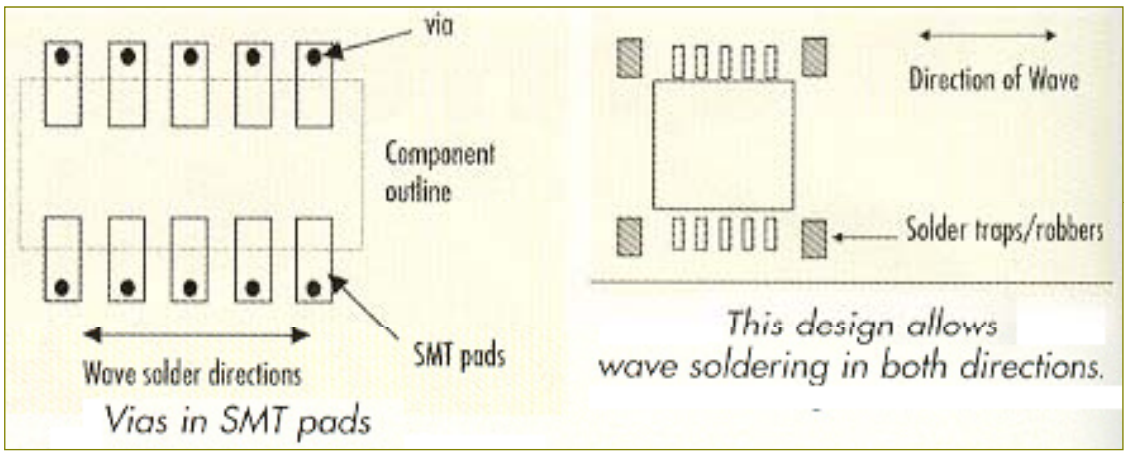
Inspect-ability Requirement



Testing After Assembly

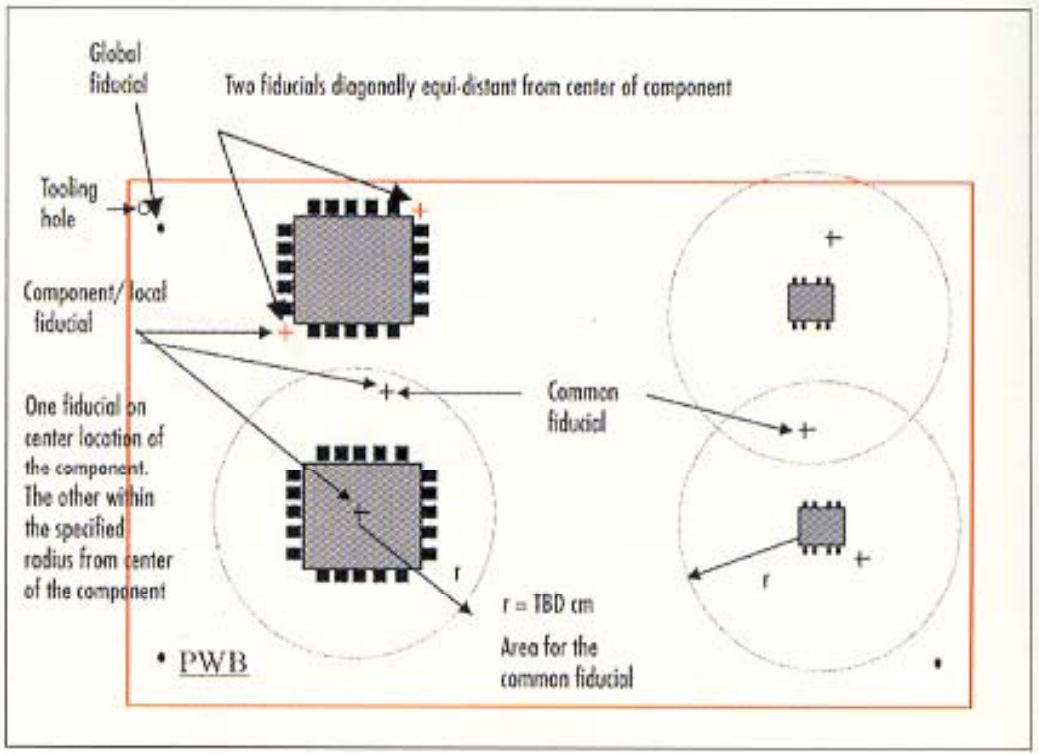


Via in SMT Pads

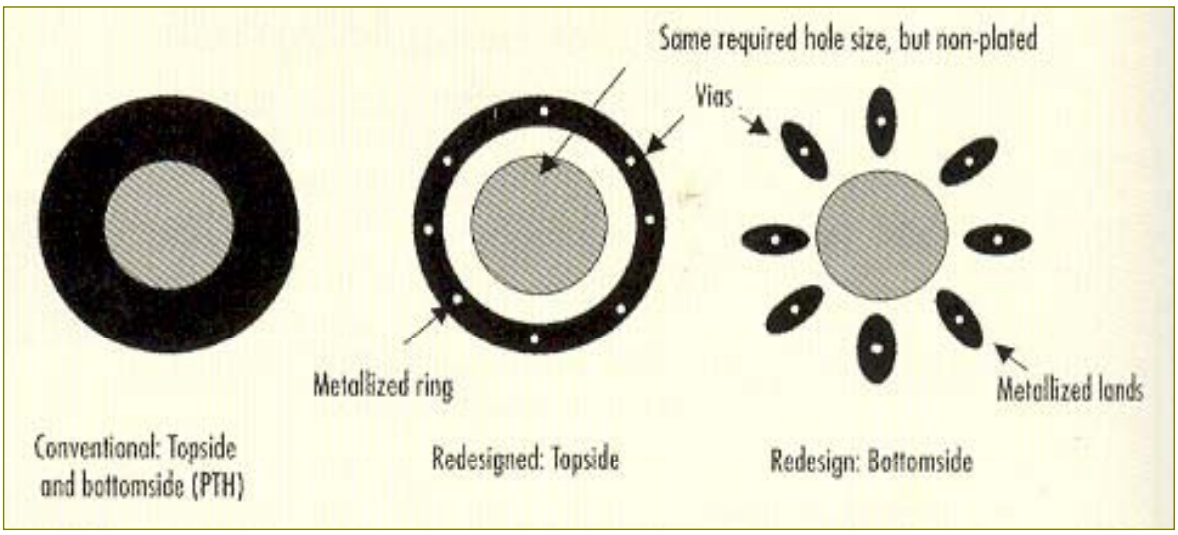


- In conventional Design via were not allowed in SMD pads (Reflow Soldering Sucks the Solder paste inside the via hole)
- In micro-via this is possible.
- Conventional Via is allowed when wave soldering is used for SMD

Local and Global Fiducials



Grounded Mounting Holes

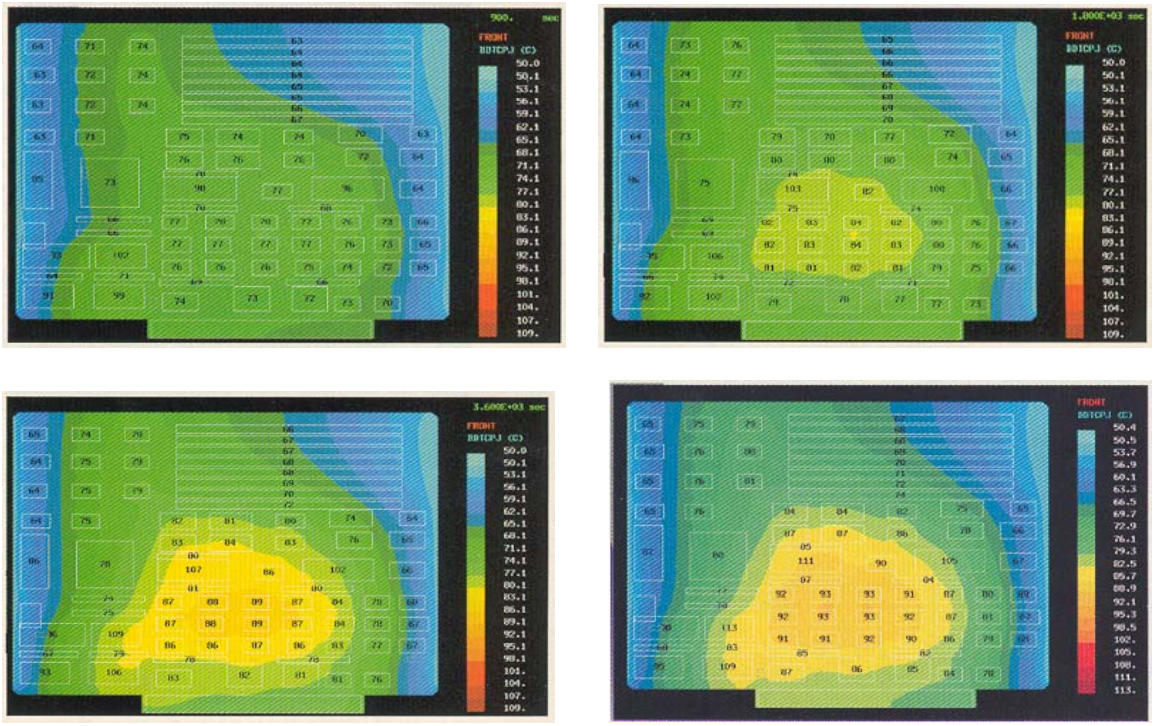


- The conventional Hole is filled by solder during Wave soldering.
- The Hole is redesigned to avoid that, but still provides the GND connection through Vias.

Thermal Analysis

- For very high/Low Temperature Environments ,the Thermal Profiling of Board is Necessary.
- For Simulation purposes simulation software's are available
- For Practical measurements THERMAL CAMERS are used with Pseudo Coloring Schemes.

@900, 1800 and 3600 S and Steady State



PCB Design Approach and Rules of Thumb

PCB Design Approach

- Life is constant balancing act between value received at what cost in time and money.
- The signal Integrity Problem is no exception, there are three ways ……..
- Rule of Thumb
  - Your intuition, order of magnitude correct answer.
- First Order Approximation
  - Quick estimate for early analysis
- Computer Simulation
  - Field Solver, SPICE and IBIS Models etc

Self inductance ~ 25 nH/inch

$$L_{self} = 5d\left[\ln\left(\frac{2d}{w+t}\right)+\frac{1}{2}\right]nH$$

Rule of Thumb-1

Band width of Signal with Rise time τ

$BW = 0.35/\tau$

Band width of CLK waveform just based on frequency

$BW = 5xF_{clk}$

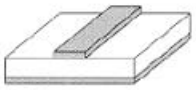
Assume rise time to be 7% of CLK frequency

Rise time τ

$\tau = 10\%F_{clk}$

Amplitude of first three odd harmonics of Square wave

0.6, 0.2, 0.12



Rule of Thumb-2

50Ω Characteristic Impedance Microstrip in FR4

W/H = 2

W = Line width

H= Dielectric Thickness

50Ω Characteristic Impedance Stripline in FR4

W/B = 1

W = Line width

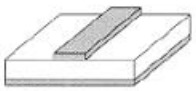
B= Dielectric Thickness between plates

Speed of Light in most Polymers

6 in/ns

Interconnect wiring delay in most Polymers

160 psec/in



Rule of Thumb-3

Maximum Length of Un-terminated Line in FR4

$L \leq 2\ t_r$

Maximum Length of Stub in FR4

$L_{STUB} \leq t_r$

Cross Talk < 3% in next FR4 Microstrip

S ≈ 3xH

S= Separation in Traces

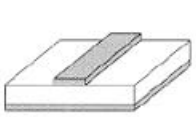
H= Thickness of Dielectric

Cross Talk < 3% in next FR4 Stripline

S ≈ 2/3xB

S= Separation in Traces

B= Total thickness of Dielectric



Rule of Thumb-4

Capacitance of 50Ω line in FR4

3.5pF/in

Inductance of 50Ω line in FR4

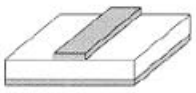
9nH/in

Maximum Capacitance discontinuity before SI problems arise

3pFx t_r (nsec)

Capacitive Load associated with Corner of Trace, 10 mil wide

20fF



Rule of Thumb-5

Maximum Inductive discontinuity before SI problems arise

9nHx t_r (nsec)

Mutual Inductance between two Traces

9nH/in

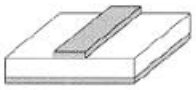
When s <length

Sheet Resistance of 1OZ of Copper

0.5mΩ/□

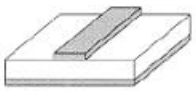
Skin Depth of Copper at 1Ghz

2 μm



Rule of Thumb-6

Maximum Inductive discontinuity before SI problems arise 9nHx t_r (nsec)	Mutual Inductance between two Traces 9nH/in When s <length
Sheet Resistance of 1OZ of Copper 0.5mΩ/□	Skin Depth of Copper at 1Ghz 2 μm



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Wakeup Please lets have Some Food….