Module-2
RF PCB Design
Microstrip Discontinuities & Simulation in Momentum

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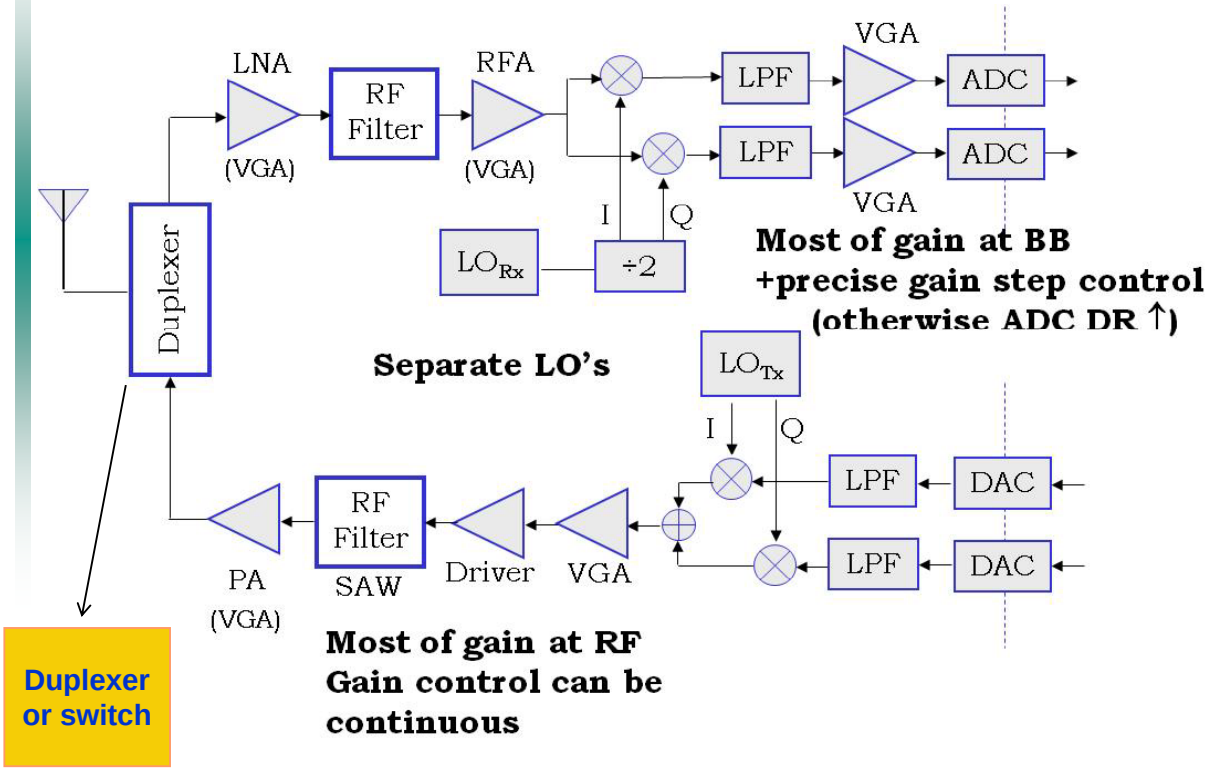
Today's Topics

- Transceiver Architectures
- TDM vs. FDM
  - Receiver Architecture
  - Transmitter Architecture
- Case Study-1: Semtech Transceiver on PCB
- Case Study-2: PA design & Layout
- Case Study-3: Patch Antenna & Layout

Overview of Standards

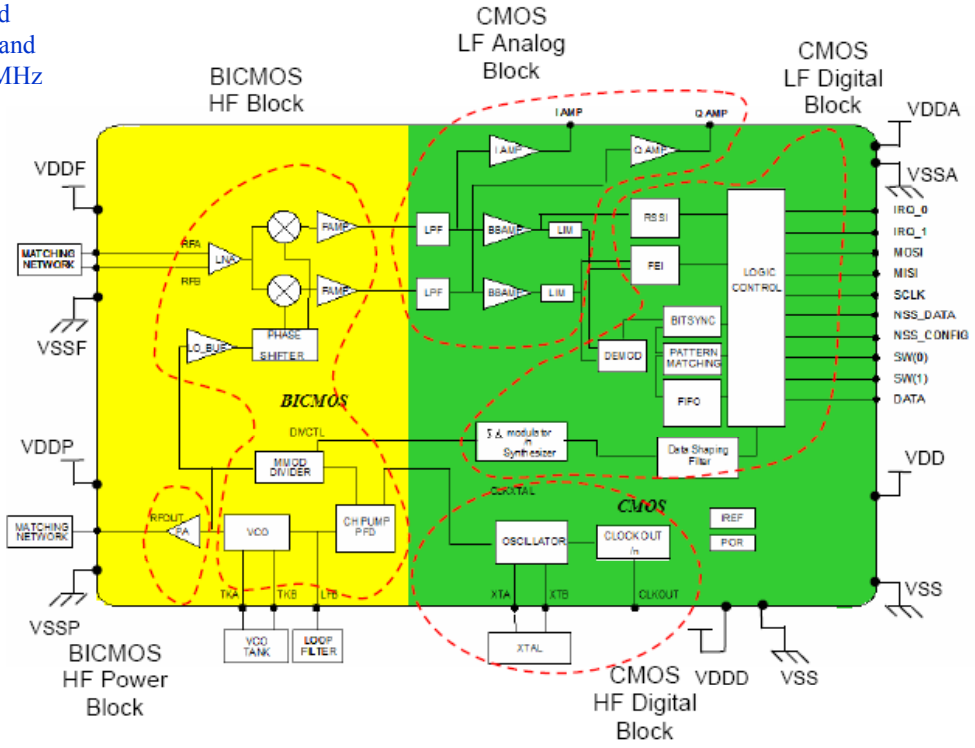
Standard	Access Scheme	Frequency band (MHz)	Channel Spacing	Frequency Accuracy	Modulation Technique	Rate (kb/s)	Peak Power
GSM	TDMA/ FDMA/ FDD	890-915 (Tx) 935-960 (Rx)	200 kHz	90 Hz	GMSK	270.8	0.8, 2, 5, 8 W
DCS-1800	TDMA/ FDMA/ FDD	1710-1785 (Tx) 1805-1850 (Rx)	200 kHz	90 Hz	GMSK	270.8	0.8, 2, 5, 8 W
DECT	TDMA/ FDMA/ TDD	1880-1900	1728 kHz	50 Hz	GMSK	1152	250 mW
IS-54	TDMA/ FDMA	824-849 (Tx) 869-894 (Rx)	30 kHz	200 Hz	$\pi/4$ QPSK	48	0.8, 1, 2, 3 W
IS-95	CDMA/ FDMA	824-849 (Tx) 869-894 (Rx)	1250 kHz	N/A	OQPSK	1228	N/A
Bluetooth	CDMA/ FDMA/FH	2400-2483	1000 kHz	20 ppm	GFSK	1000	1,4,100 mW
802.11b (DSSS)	CDMA	2400-2483	20 MHz	25 ppm	CCK	11 Mb/s (max)	1 W
FDD UMTS TDD UMTS	FD-CDMA TD-CDMA	1920-1980 (Tx) 2110-2170 (Rx) 1900-1920 (TDD)	5000 kHz	0.1 ppm	QPSK QAM	2 Mb/s 10 Mb/s	0.125, 0.25, 0.5, 2W

RF Transceiver Architecture..



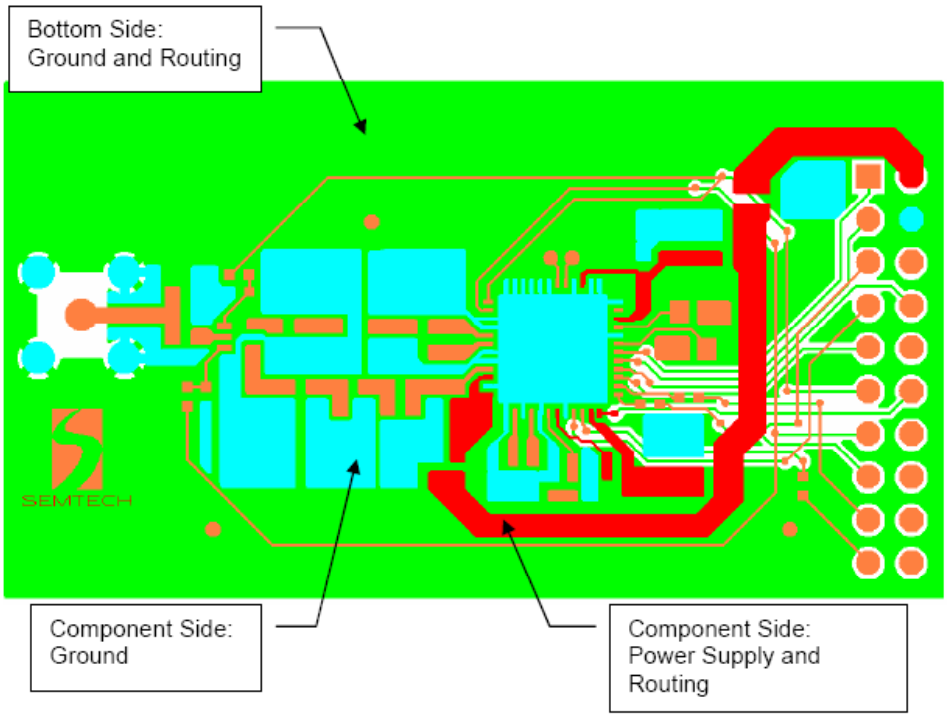
SEMTECH ISM Band Transceiver

The industrial, scientific and medical (ISM) Band.
Bluetooth 2450 MHz band
HIPERLAN 5800 MHz band
IEEE 802.11/WiFi 2450 MHz
& 5800 MHz bands

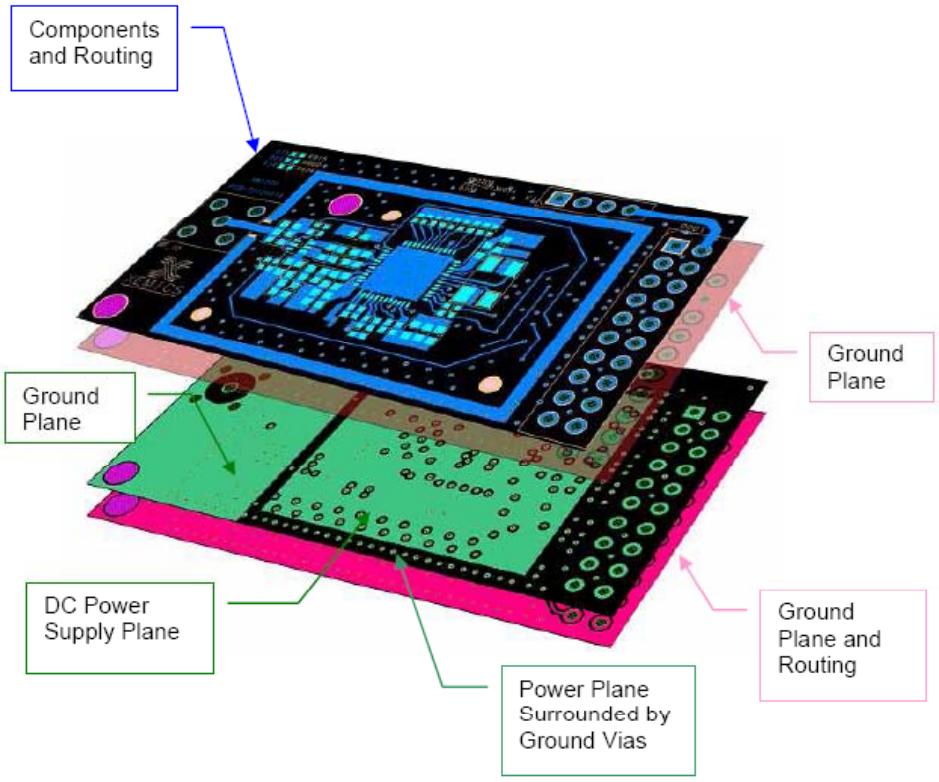


2-Layer Stackup

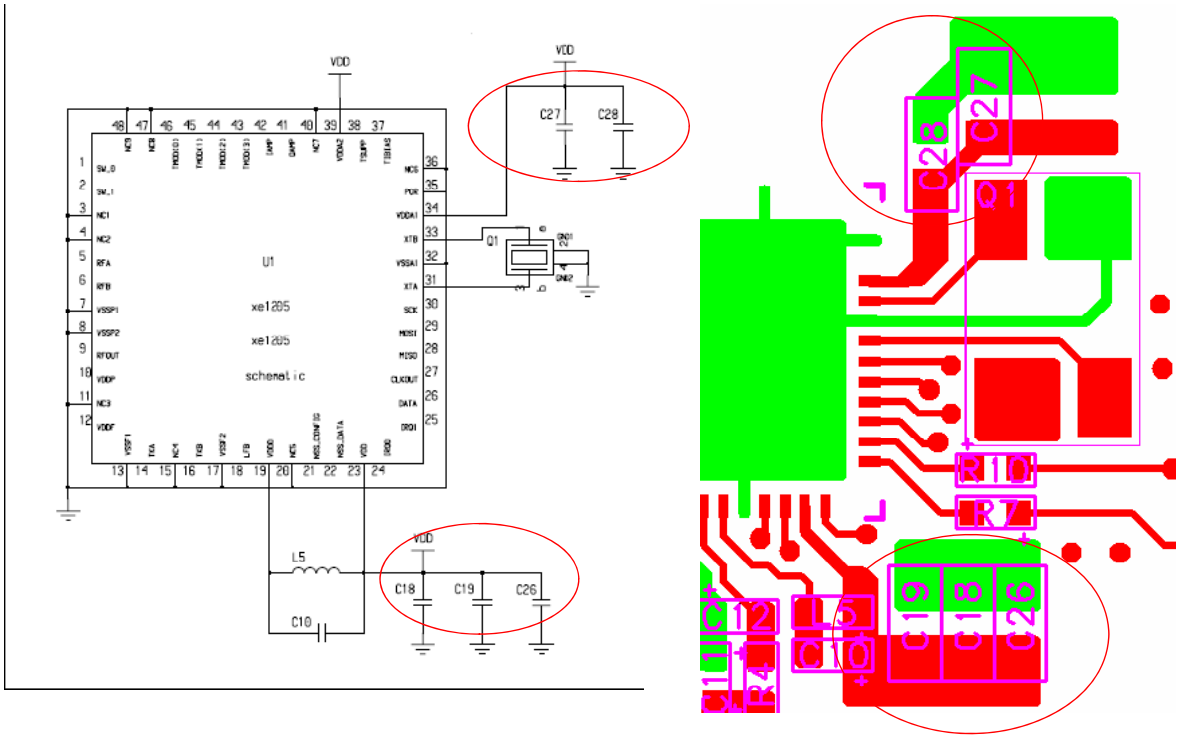
•A 2-layer PCB will be cheaper to than a 4-layer PCB.
•To implement Microstrip or Stripline the PCB thickness should not exceed 0.8mm - 1.00mm (0.031" -0.039"),
•The width of the transmission line trace will become rather large.



4-Layer Stackup

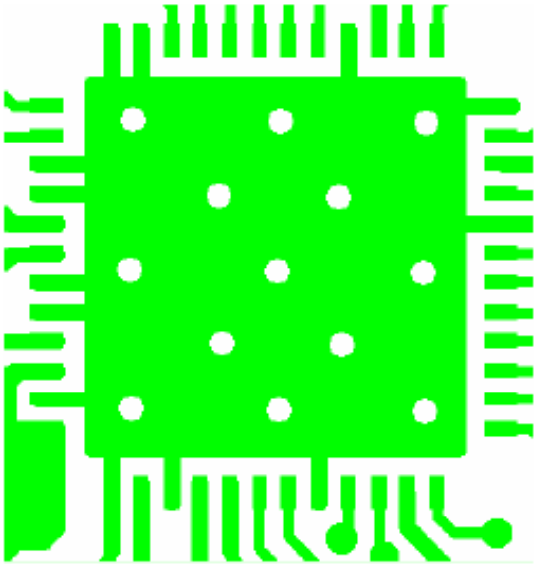


Decoupling Capacitors



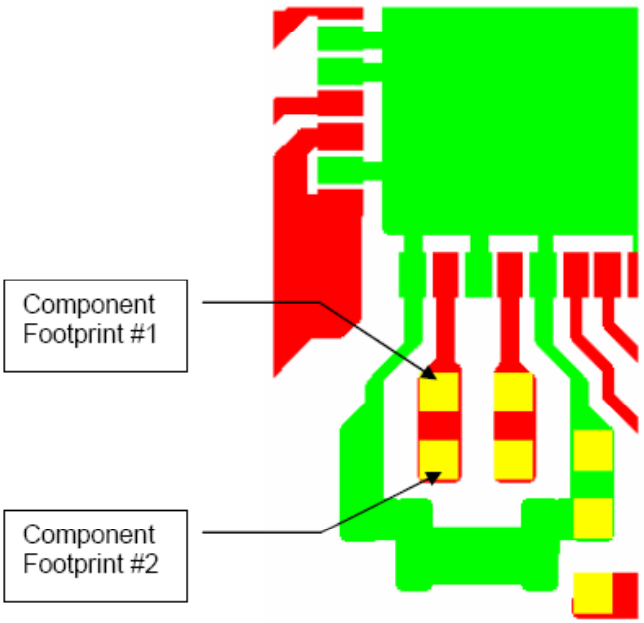
Thermal Relief Vias

- The thermal relief pad on the underside of Semtech RF devices provides both thermal relief and a solid ground reference to the chip
- Well stiched through vias to the GND plane on the other side



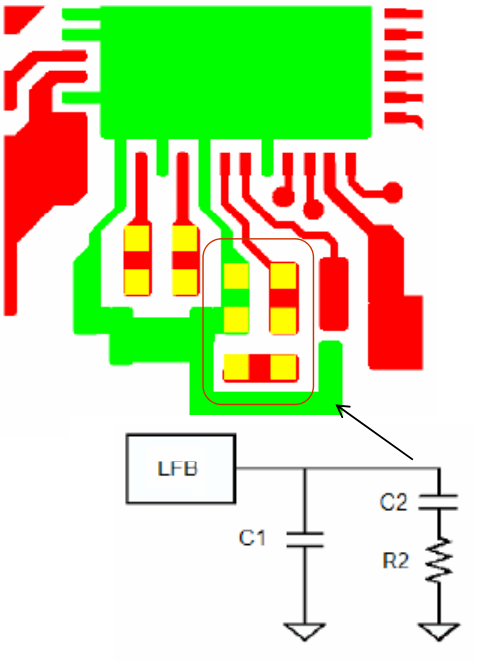
VCO L and C

- Symmetrical PCB layout of the XE1200 series VCO tank.
  - Short Traces
  - Ground guard band
  - Inductor should be placed orthogonal to the PCB trace for low coupling



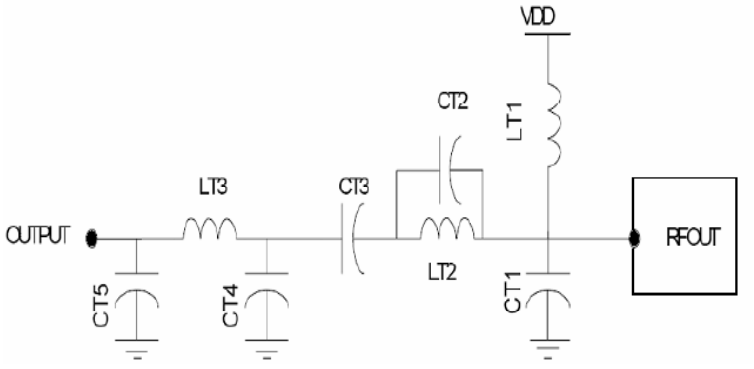
PLL Loop Filter

- Noise Injected in the loop will appear as FM noise
  - Small loop area as possible
  - Guard trace around the component
  - Traces parallel



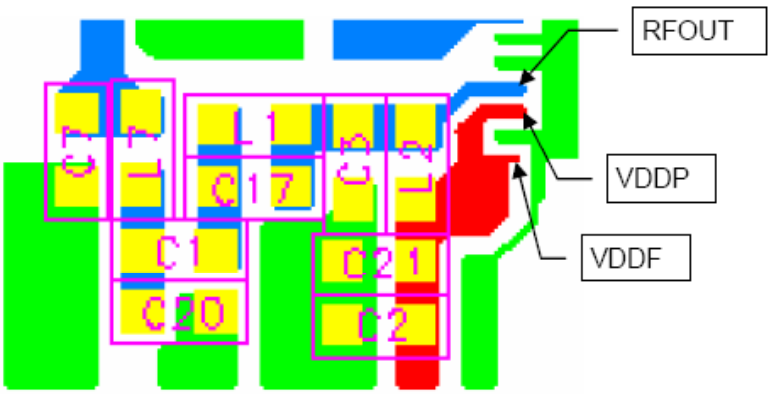
XE120x: Second Order Loop Filter

Transmitter Matching and Filtering



- LT1, CT1: Together with both PCB and device (packaging) parasitic forms a resonant load atthe required output frequency.
- LT2, CT2: For applications that need to comply with the requirements of ETSI EN 300 220, this network forms a band stop filter resonant at the second harmonic.
- CT3 provides a DC block.
- CT4, CT5, LT3: Form a low-pass harmonic filter.

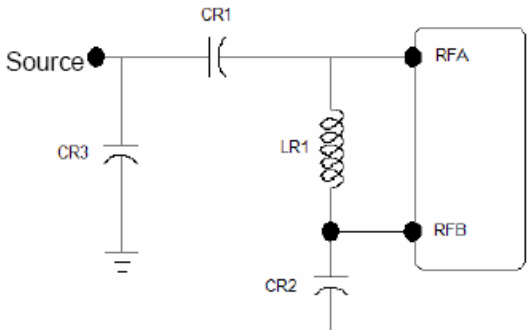
Transmitter Decoupling

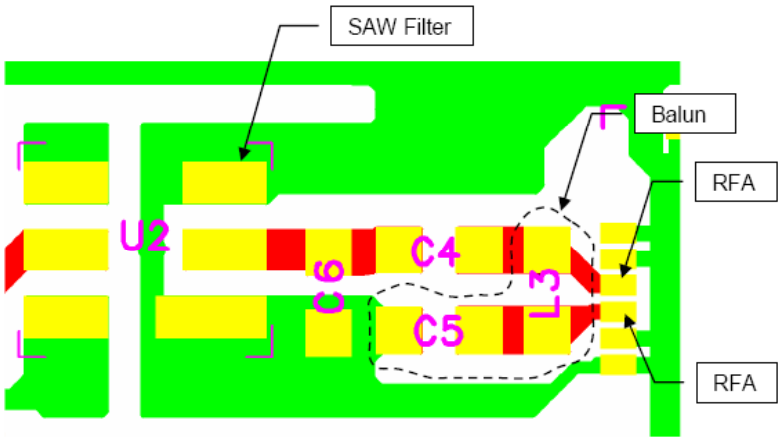


- The power supply to both the transmitter (VDDP) and the RF block (VDDF) are decoupled by **C21 and C2.**
- The Load inductor, L2, is placed at right-angles to the VCO tank inductor and L1 to minimize inductive coupling. The circuit layout does not fold back upon itself so as again to minimize cross-coupling.

LNA Matching Network

- CR2 and LR1, to provide 180° phase shift to the differential input ports of the LNA at RFA and RFB.
- CR1 and CR3 (where required) to provide the impedance transformation and matching to the source impedance (nominally 50ohms).

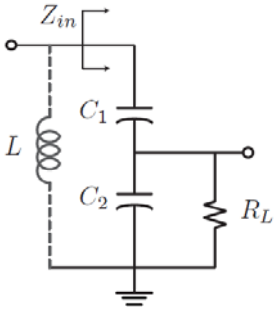




Impedance Matching using C&C

$$Z_{in} = \left[\frac{1/j\omega C_2 \times R_L}{1/j\omega C_2 + R_L}\right] + 1/j\omega C_1$$

$$Z_{in} = \left[\frac{R_L}{1 + j\omega R_L C_2}\right] + 1/j\omega C_1 = \frac{j\omega R_L C_1 + (1 + j\omega R_L C_2)}{j\omega C_1 - \omega^2 R_L C_1 C_2}$$



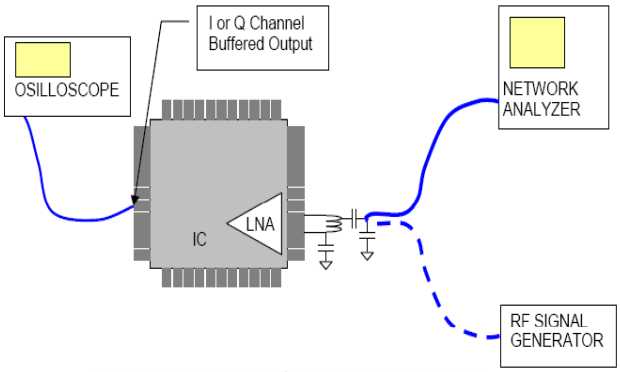
$$Y_{in} = j\omega C_1 \times \frac{1 + j\omega R_L C_2}{1 + j\omega R_L (C_1 + C_2)}$$

$$\mathrm{Re}[Y_{in}] = G_{in} = \frac{\omega^2 R_L C_1^2}{\omega^2 R_L^2 (C_1 + C_2)^2 + 1}$$

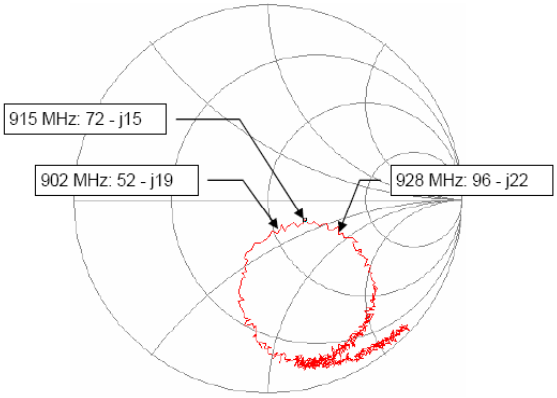
$$\omega >> \frac{1}{R_L (C_1 + C_2)} \Rightarrow \quad G_{in} \approx \frac{C_1^2}{R_L (C_1 + C_2)^2} \Rightarrow$$

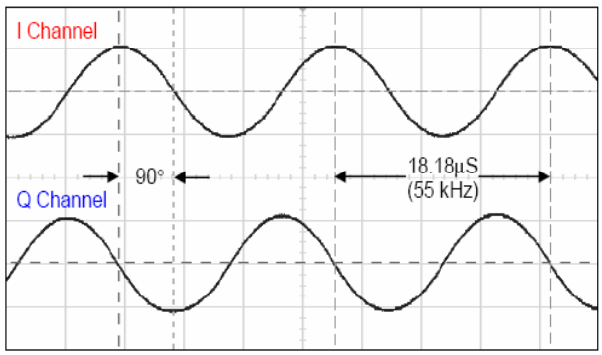
$$R_{in} \approx R_L \left(\frac{C_1 + C_2}{C_1}\right)^2$$

Input Match Optimization



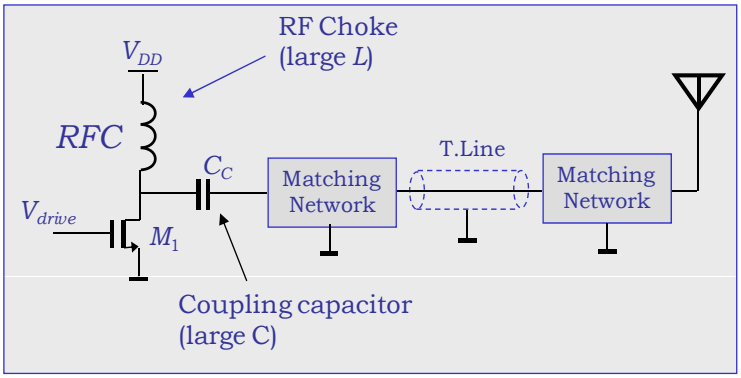
RF Signal Level (dBm)	I, Q Channel Signal Level (mV_{pp})
-50	2650
-60	2500
-70	1300
-80	500
-90	150
-95	90
-100	45
-105	30





Case Study-2
Power Amplifier Design

Case Study: Power Amplifier



Example:

$P_A = 1W$ at 50Ω then $V_A = 50^{1/2}V$

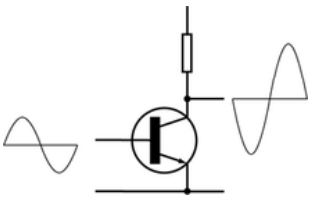
$V_{A,pp} = 20V$ large voltage swing needed at 50Ω

But max. swing at PA output: only $2V_{DD}$,

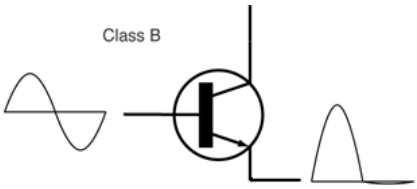
If $2V_{DD} < V_{A,pp}$ then downwards impedance conversion needed

We provide the amount of power needed by the antenna

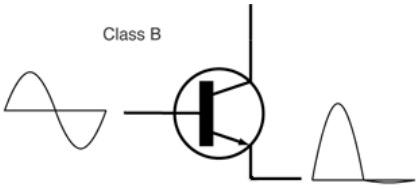
Power Amplifier Classes



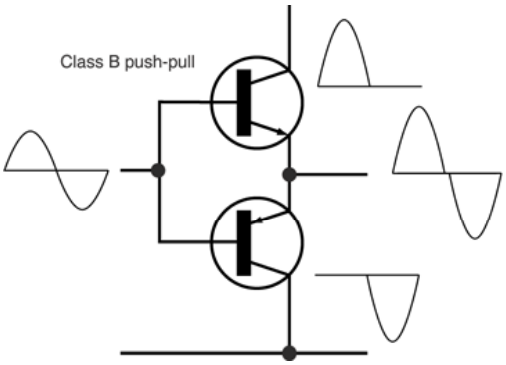
Class-A
100%

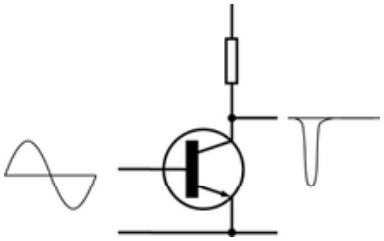


Class-B
50%



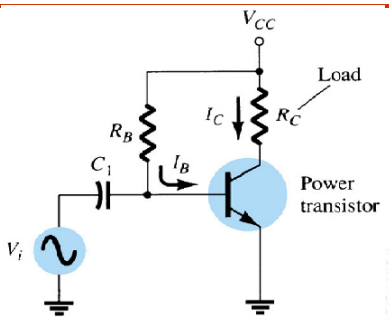
Class-AB
+50%

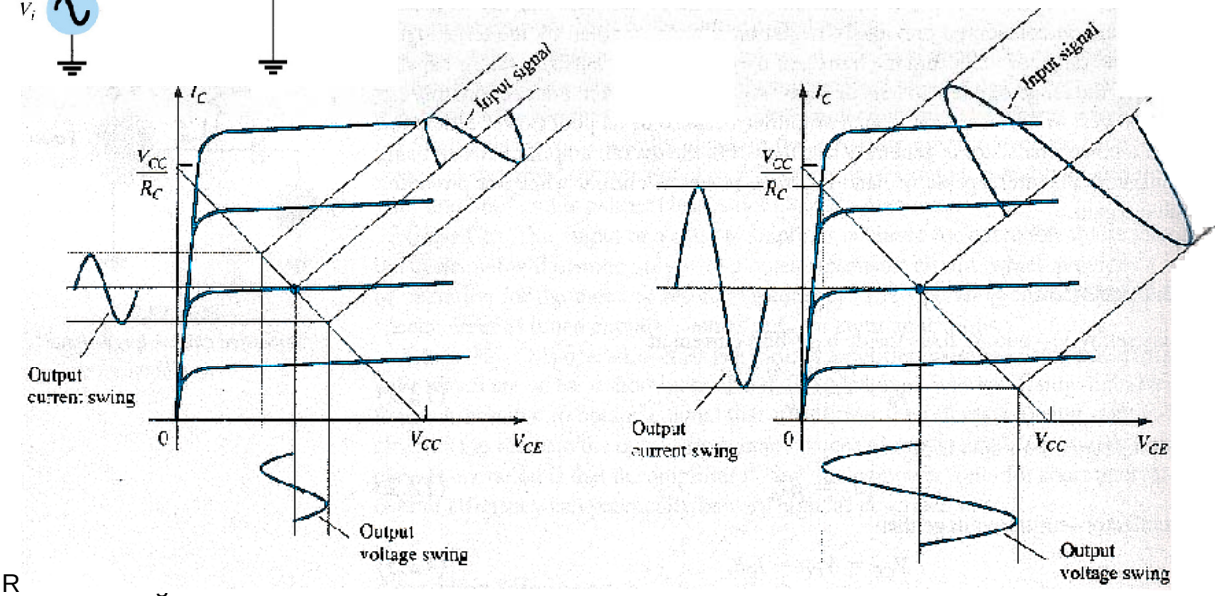




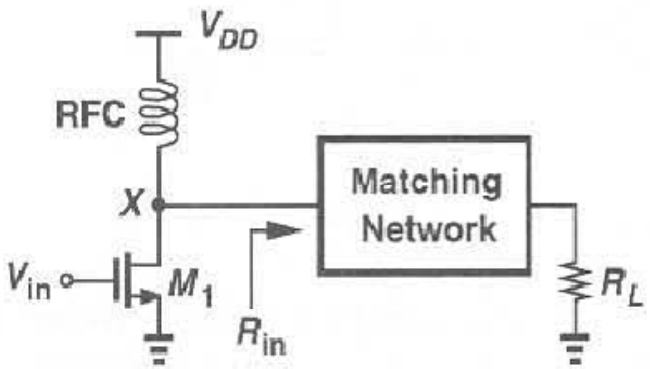
Class-C
<50%

DC Bias & Load Line





Simplified Class-A PA



Load Line of Class-A PA

$$P_0 = \frac{|V_0|^2}{R_0}\bigg|_{\substack{\text{atmax}\\ \text{swing}}} = \frac{V_{DD}^2}{2R_0}, \text{ and } P_{DC} = V_{DD} I_{L0}$$

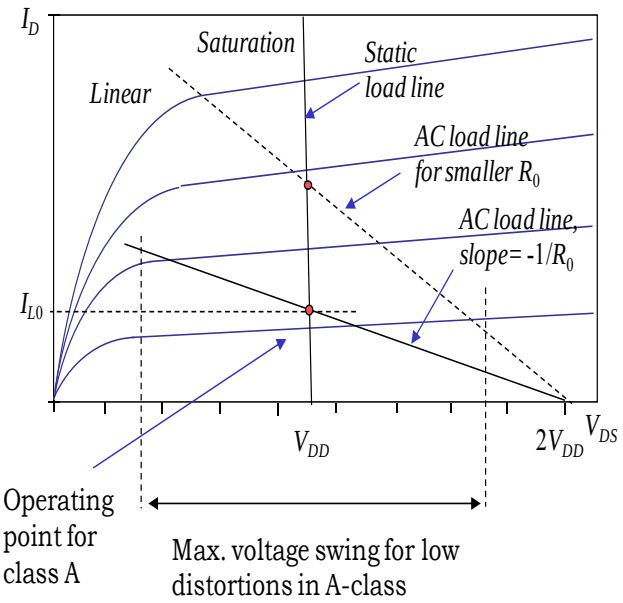
$$I_{0m} = |I_0|\sqrt{2}\,\Big|_{\substack{\text{atmax}\\ \text{swing}}} = I_{L0}$$

$$P_{DC} = V_{DD} I_{L0} = V_{DD} I_{0m} = \frac{V_{DD}^2}{R_0}$$

$$\eta = \frac{P_0}{P_{DC}}\bigg|_{\substack{\text{atmax}\\ \text{swing}}} = \frac{1}{2}$$

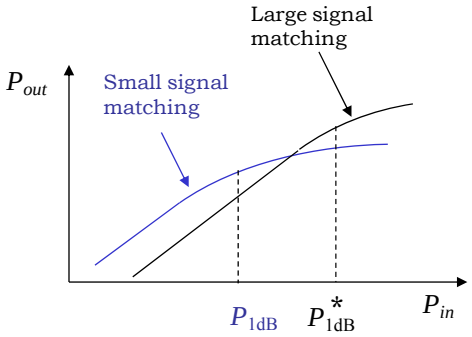
Power efficiency (drain efficiency)

But in practice only < 35%

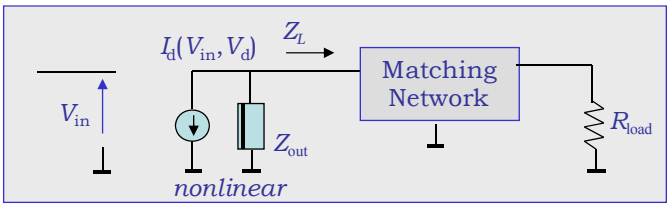


Large Signal Impedance Matching

- Power matching and efficiency are contradictory
- Classical matching for power would degrade efficiency
- Large signal matching by load-pull test preferred

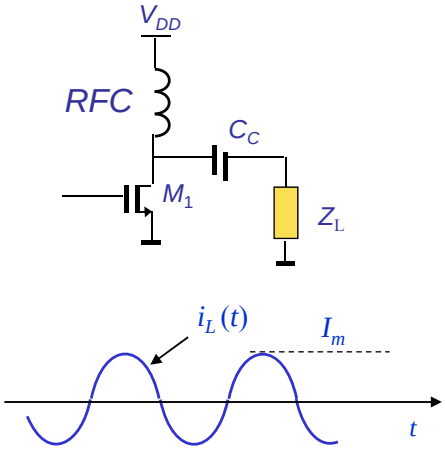


Large signal matching tends to provide largest dynamic range



Matching Z_L for low enough resistance R_L, and cancellation of X_{out} (to reduce the reactive current) must be done over the range of amplitudes – difficult modeling task with accurate transistor models (Load-pull test) Parasitics play role !

Load Pull Test



Assume A class amplifier

If parasitics are neglected: $Z_L = R_{opt} = V_{DD}/I_m$
and $P_{opt} = (I_m)^2 R_{opt}/2$ and $I_m = I_{bias}$

Now assume $Z_L = R_L + jX_L$ so $P_L = (I_m)^2 R_L/2$ and
$(V_m)^2 = (I_m)^2 [(R_L)^2 + (X_L)^2]$

In current mode we need $V_m < V_{DD}$ (to avoid distortion)

so $(R_L)^2 + (X_L)^2 < (R_{opt})^2$

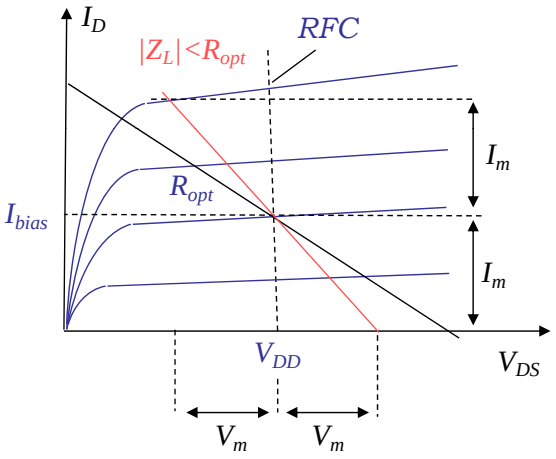
Otherwise: $(R_L)^2 + (X_L)^2 > (R_{opt})^2 \Leftrightarrow (G_L)^2 + (B_L)^2 < (G_{opt})^2$

so $P_L = (V_{DD})^2 G_L/2$ in "voltage mode"

and $(I_m)^2 = (V_{DD})^2 [(G_L)^2 + (B_L)^2]$ but also $I_m < I_{bias}$

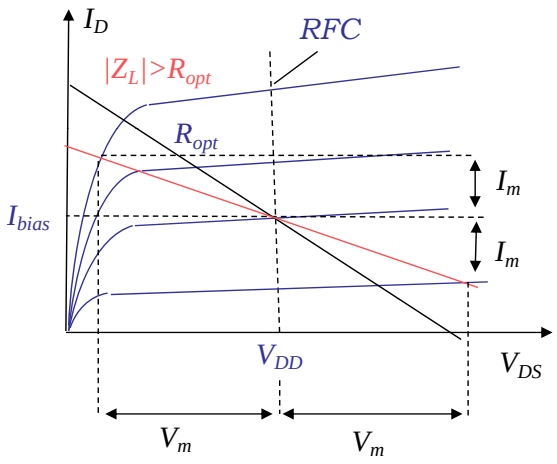
This is only a linear model and also MOSFET parasitics are missing

Load Pull Test



Current mode

$I_m \approx I_{bias}$ and $V_m < V_{DD}$



Voltage mode

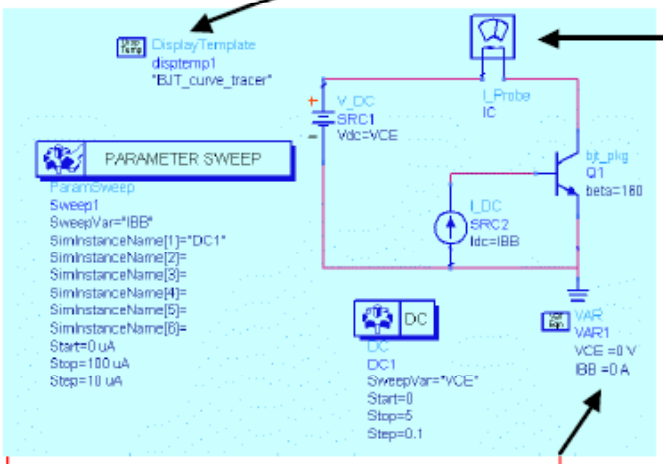
$V_m \approx V_{DD}$ and $I_m < I_{bias}$

PA Design Using ADS

1. DC Simulation and Bias Point Selection
2. S-Parameters and Optimization
3. Harmonic Balance Simulations (Optional)
4. Circuit Envelope Simulation (Optional)
5. Filters - Trans, Design Guide, Momentum
6. Final Circuit & System simulations

DC Bias Point Selection

This template also has a data display template.

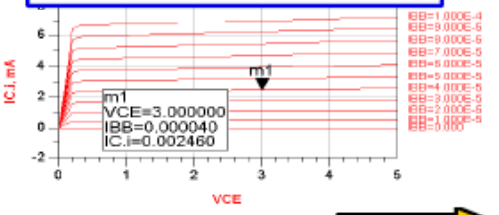


Probe give current current in dataset.

Your model (**bjt_pkg**) with annotation and passed parameter: beta.

Initialized VARs: VCE=0V & IBB=0A

Data Display template gives curve tracer results:



NOTE: DC controller sweeps the X-axis and the Parameter Sweep, sweeps the Y-axis.

S-Parameters

S-parameter ratios: *S out / S in*

- S11 - Forward Reflection (input match - impedance)
- S22 - Reverse Reflection (output match - impedance)

Best viewed on a Smith chart (next slides).

- S21 - Forward Transmission (gain or loss)
- S12 - Reverse Transmission (leakage or isolation)

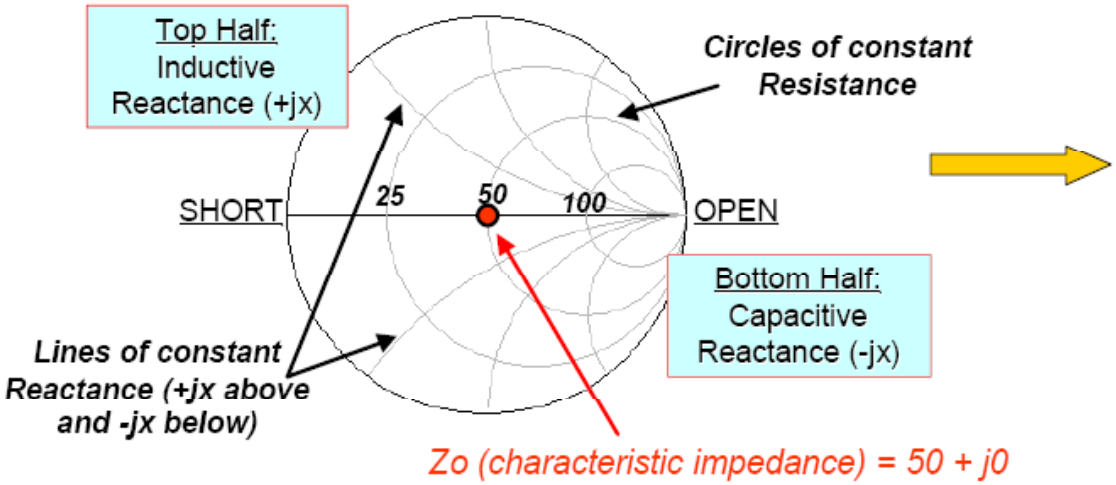
These are easier to understand and simply plotted.

Results of an S-Parameter Simulation in ADS

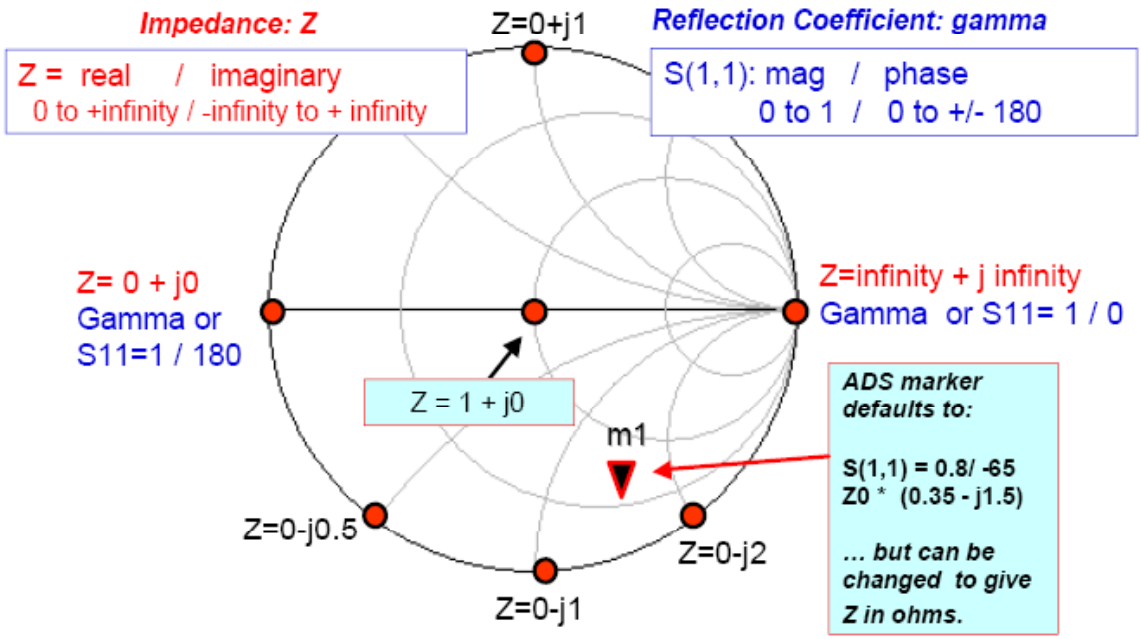
- S-matrix with all complex values at each frequency point
- Read the complex reflection coefficient (Gamma)
- Change the marker readout for Zo
- Smith chart plots for impedance matching
- Results are similar to Network Analyzer measurements

Perfect Impedance Point

This is an impedance chart transformed from rectangular Z.
Normalized to 50 ohms, the center = R50+J0 or Zo (perfect match).
For S11 or S22 (two-port), you get the **complex impedance**.



Perfect Impedance Point

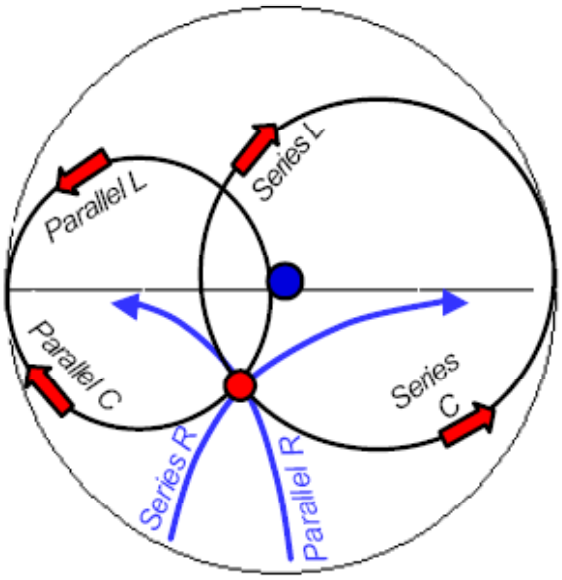


Moving Towards the Centre

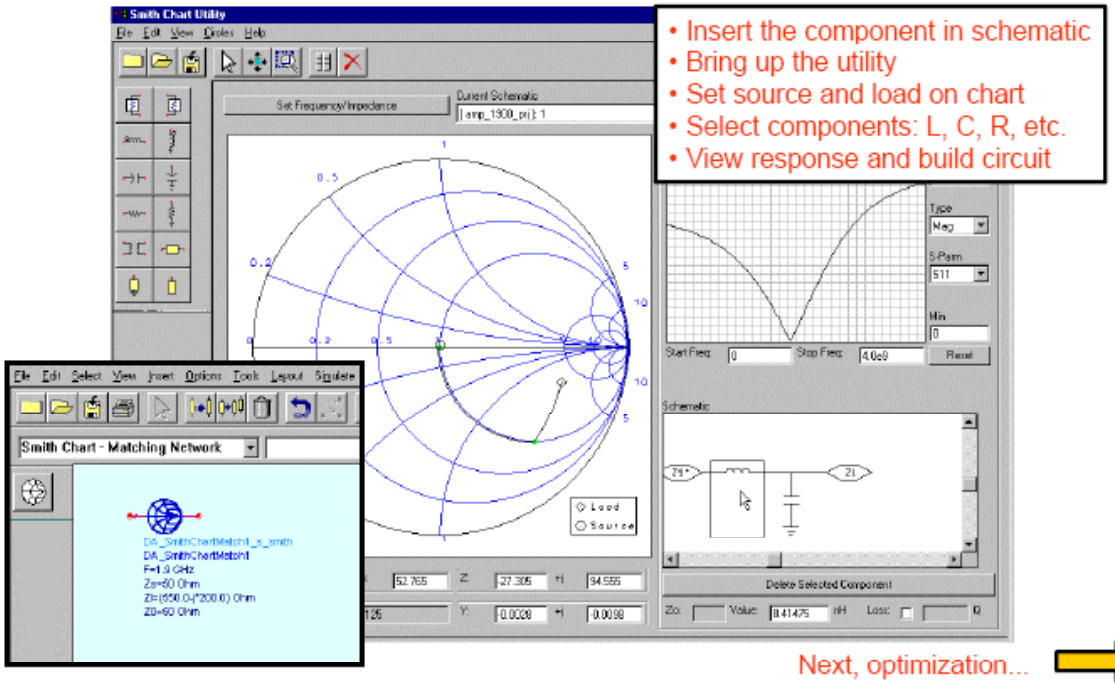
Add Series or Parallel (shunt) components.

You will do this in the lab.

Adjust the value to move toward open, short, L, C, or center of chart.



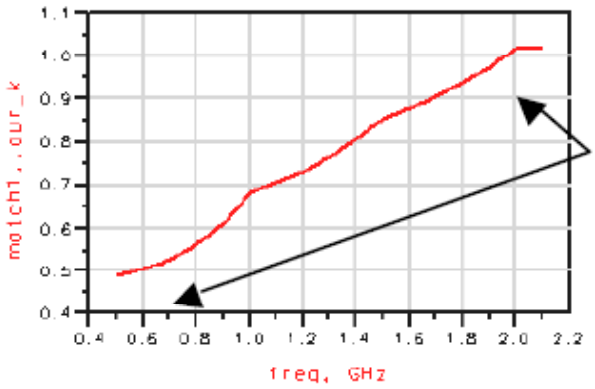
Smith Chart Optimization Utility



- Insert the component in schematic
- Bring up the utility
- Set source and load on chart
- Select components: L, C, R, etc.
- View response and build circuit

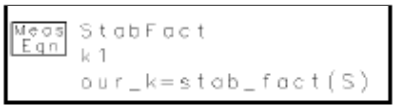
Next, optimization...

Stability-factor K



Area of low Frequency conditional stability (0<K<1.0) indicates need for adding a stabilization network.

Use measurement equation from ADS S-parameter palette →



K-factor that is greater than one tells you that your amplifier is unconditionally stable.
If K is less than 1, you may have a problem. Below is the equation for K-factor:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

Stability-factor K

- Large power Transistor have very high transconductance, leading to potentially high gain at low frequencies. This high low frequency gain can cause stability problems.
- To reduce the gain at low frequency, we can add the stability circuit, which is usually simple RC combination in series with transistor input.

Gain, In/Output Matching

S-parameter ratios: *S out / S in*

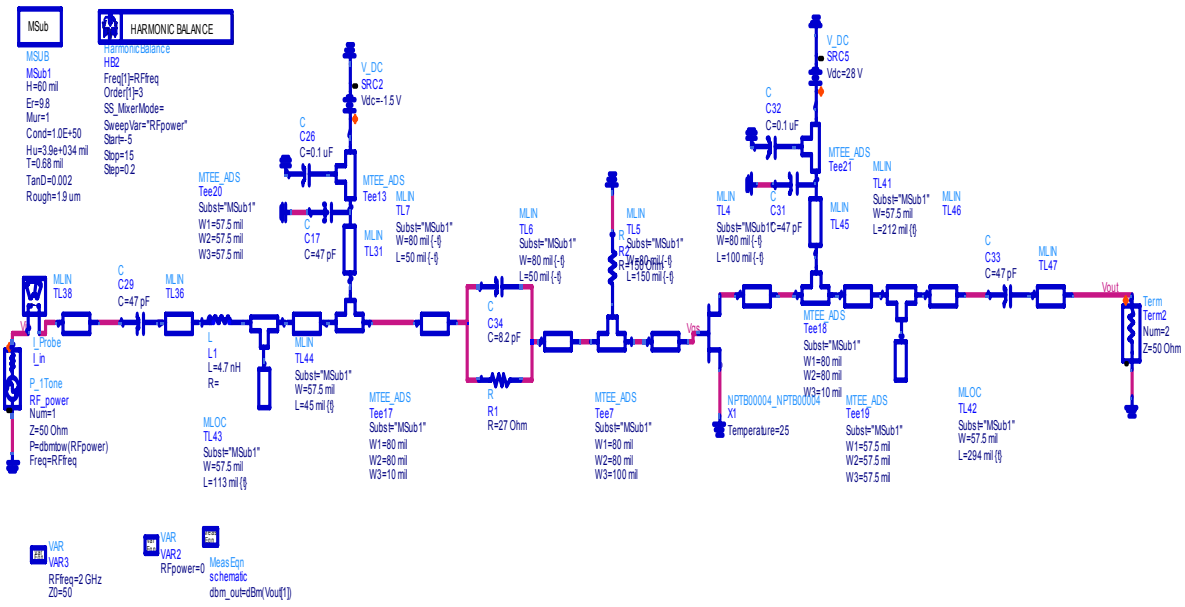
- S11 - Forward Reflection (input match - impedance)
- S22 - Reverse Reflection (output match - impedance)

} Best viewed on a Smith chart (next slides).

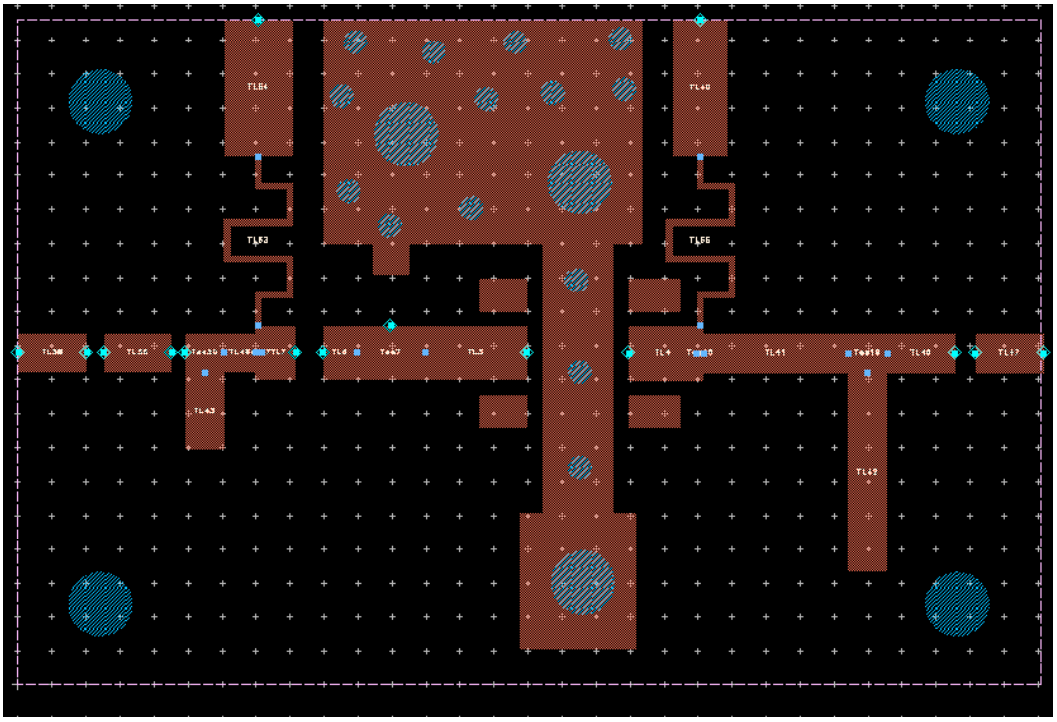
- S21 - Forward Transmission (gain or loss)
- S12 - Reverse Transmission (leakage or isolation)

} These are easier to understand and simply plotted.

Final Schematic



Final Circuit



What Left….

- An Antenna
- In LAB we will learn to design 50Ω patch antenna to be used with PA.

Summary

- Case Study-1: Semtec Transceiver on PCB
- Case Study-2: PA design & Layout
- Case Study-3: Patch Antenna & Layout