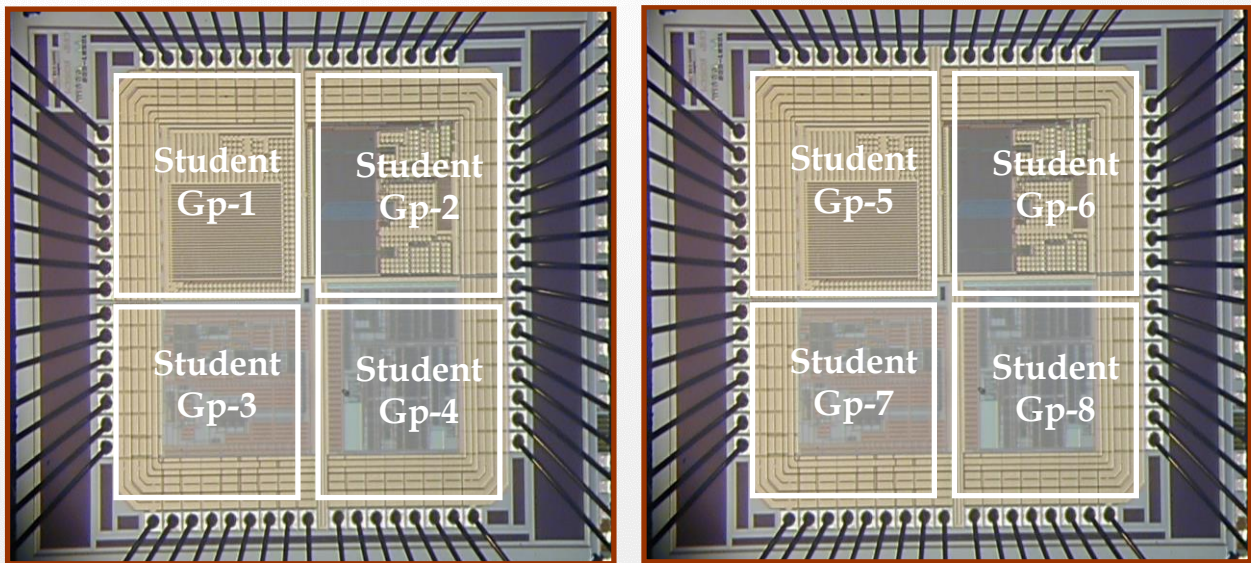


# IC Design Project Hand Book

65nm CMOS TSMC  
Expected Tapeout Spring 2021



**“A Training from Idea to Product Design”**

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**Program Aims and Objectives:**

- **Hands on IC Design Experience:** Extensive hands on Si tape out experience from concept to the real world working silicon.
- **Seeding the Innovation:** to provide a guided and mentored path for students to find the solution of an IC design problem in a unique and innovative way.
- **Research Methodology:** Locating, accessing, efficient reading and then the understanding the published material and learn to learn the state-of-art in the particular area of the research.
- **Learning from Giants:** Provision of the opportunities to talk to the IC design and learn the confidence and latest techniques and knowledge.
- **Publishing the work:** To give them the confidence that you by publishing in the high quality journals and conferences like IEEE JSSC and ISSCC. This will give the students an immense self-confidant for the future projects.
- Expected tapeout Date: 30 July, 2021
- The estimated cycle-time is 62 days from tapeout to shipment.

*Note-1:* Each project team will design its own PCB after the PAD frame and pad functions are decided on 29 March, 2021.

*Note-2:* The mm-wave projects will be measured using the on-chip wafer probing or the direct bond wiring on Rogers PCB.

*Note-3:* All other project will use the QFN package mounted on the FR4 or Rogers PCB depending upon the frequency of application and type of the circuit.

**Proposed Projects:**

These projects are proposed keeping in view that they are implementable:

- In one semester from schematic/RTL to the GDS generation with the team of 3 to 4 students.
- Have an element of the innovation in each project so that they are easily publishable.

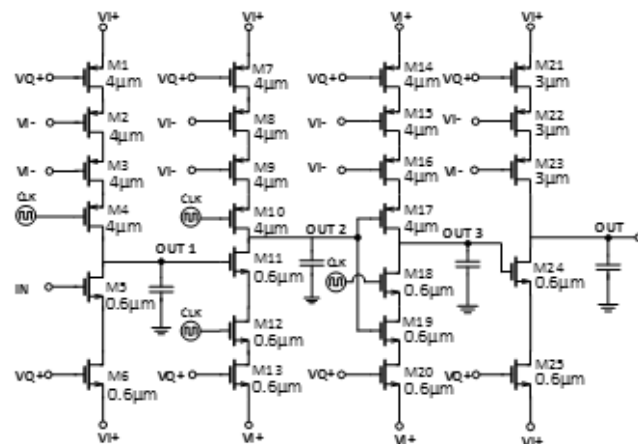
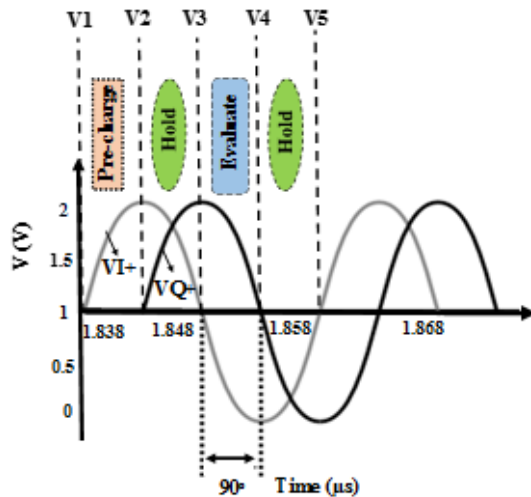
Activity		Main Area
1	Logic Family with AC Supply Voltage for Self-Powered Digital ASICs	Digital
2	Fault Tolerant CLB Design for High Reliability Autonomous Applications	Digital
3	28-32 GHz LNA for 5G NR applications	Analog RF
4	mm Wave Phase Shifter for MMIMO Application	Analog RF
5	MMIMO Channel Estimation with Low-Resolution Spatial Sigma-Delta ADC	Mix Signal
6	Capacitor-less High Efficiency Triboelectric Energy Harvester	Mix Signal
7	ASIC Implementation of ALU based on Approximate Computing Techniques	Digital
8	Oscillator based True Random Number Generator for 5G NR Applications	Digital

### Project-1: Logic Family with AC Supply Voltage for Self-Powered Digital ASICs

The IoT is an emerging field with a huge commercial potential. The IoT aims to solve the problems in diverse fields, such as implantable devices, global health care, smart cities, food and agriculture, environmental monitoring. The self-powering capability makes it possible for the IoT ASICs to work for decades; the same is true for the implantable biomedical sensors.

The specialized single-chip CMOS ASIC designed for energy harvesting, it is possible to harvest in the order of a few micro-watts. The on-chip CMOS transistors used in rectification are usually quite large in order to reduce the resistive power loss where received power signals are low in amplitude and the CMOS threshold voltages are high resulting in very low-efficiency rectification. In this project we will study the existing design powering the CMOS logic circuits directly with AC-signals without in DC supply voltage.

We have to come up with the new logic cell design using the Quadrature (I and Q) *RF-only signals* logic for designing the self-powered WPT Digital CPU. The QRF-only logic will not require the low efficiency RF-to-DC rectifier block therefore boosting the power-efficiency while reducing the chip area.



**Skill Development:** Digital Logic Design, WPT System Design, Ultra Low Power sub Threshold logic design techniques, Dynamic Logic

**Application Areas:** Implantable Medical Devices, IoT Smart Dust and Self Powered Sensors and Systems

**Innovation Aspects:** ★★★★★ (5/5) [Extremely high], no known design exists.

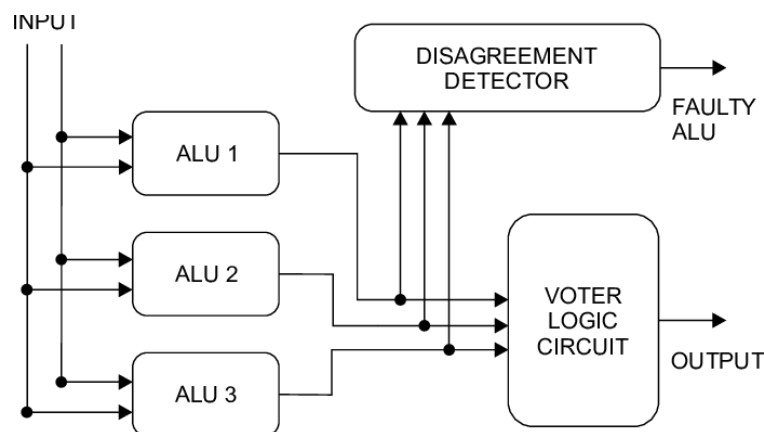
#### References:

1. Dr. Rashad Ramzan unpublished work. (will be provided)
2. J. Wenck, R. Amirtharajah, J. Collier, and J. Siebert, "AC power supply circuits for energy harvesting," in Proc. IEEE Symp. VLSI Circuits, Kyoto, Japan, Jun. 2007, pp. 92–93.
3. A. G. Dickinson and J. S. Denker, "Adiabatic dynamic logic," IEEE J. Solid-State Circuits, vol. 30, no. 3, pp. 311–315, Mar. 1995.

## Project-2: Fault Tolerant CLB Design for High Reliability Autonomous Applications

As the device size decreases, the reliability degradation caused by soft-errors and multiple component error due to a single soft-error are becoming serious problems in VLSI systems.

Configurable Logic Blocks (CLBs) are basic building blocks in FPGAs. For modern commercially available FPGAs the internal architecture of CLBs is generally kept hidden, however patents and scholarly articles suggest some of highly practical implementations. These designs can further be modified to add novelty and reliability and the ASICs can be used as test platform. A single or plurality of CLBs could be integrated in to the proposed design along with a limited test circuit



**Skill Development:** Verilog HDL, Logic Design, Digital Design, FPGA architecture, ASIC development

**Innovation Aspects:** ★★★★★ (4/5)

**Application Areas:** Low Power Microprocessor Design, Reliable error free Processor for Autonomous vehicles, UAV applications, and medical instrumentations

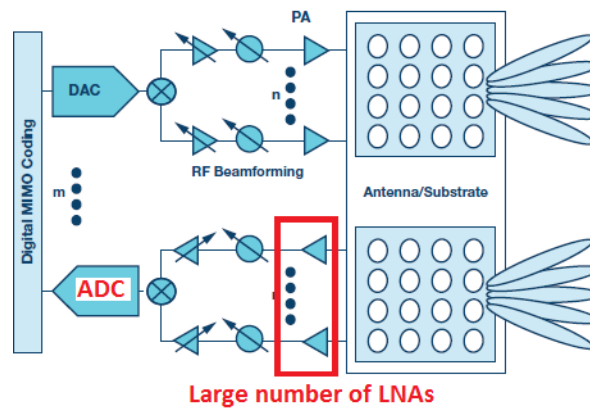
### References:

1. Shukla, Satyam, and Kailash Chandra Ray. "Design and ASIC Implementation of a Reconfigurable Fault-Tolerant ALU for Space Applications." 2019 IEEE International Symposium on Smart Electronic Systems (iSES)(Formerly iNiS). IEEE, 2019.
2. Krištofík, Štefan, Marcel Baláž, and Peter Malík. "Hardware redundancy architecture based on reconfigurable logic blocks with persistent high reliability improvement." Microelectronics Reliability 86 (2018): 38-53.
3. Kourfali, Alexandra, Amit Kulkarni, and Dirk Stroobandt. "SICTA: A superimposed in-circuit fault tolerant architecture for SRAM-based FPGAs." 2017 IEEE 23rd International Symposium on On-Line Testing and Robust System Design (IOLTS). IEEE, 2017.
4. Wilson, Christopher, et al. "Hybrid, adaptive, and reconfigurable fault tolerance." 2017 IEEE Aerospace Conference. IEEE, 2017.

### Project-3: 28-32 GHz LNA for 5G NR applications

As the development of 5G/6G wireless networks continues, the performance of the front end of a radio is an increasingly critical element in the RF receiver signal path, particularly with respect to the LNAs. If the LNA performance falls short, the remaining design efforts in circuit will be of no help as this is the first amplification element in the receiver chain.

For 5G, especially approaching 28 GHz, the NF generally needs to be between 1 and 3 dB, and P1dB and output 3<sup>rd</sup> order intercept (OIP3) need to be at least -20 and -35 dBm, respectively. This has to be achieved without few or no inductor to save the chip area. There might be 64 or more LNAs on one chip. The classic LNA topologies do not meet these requirements. There is immense room for the innovation at this point. Since all the system component are on chip, low power consumption is an extremely important aspect and it becomes a big challenge to improve the noise performance in low power regime



**Skill Development:** Extreme Amplification at mm-Wave Analog and RF Circuit Design, mm-Wave Circuits, Signal Integrity, CMOS transistor modeling, Extreme Layout Optimization, Impedance Matching,

**Innovation Aspects:** ★★★★★ (4/5)

**Research Areas:** 5G/6G Receivers, MIMO Receiver, mm-wave receivers

**Application Areas:** 5G/6G Receivers, Phase Array Radars, Low Power Future Satellite Receivers

#### References:

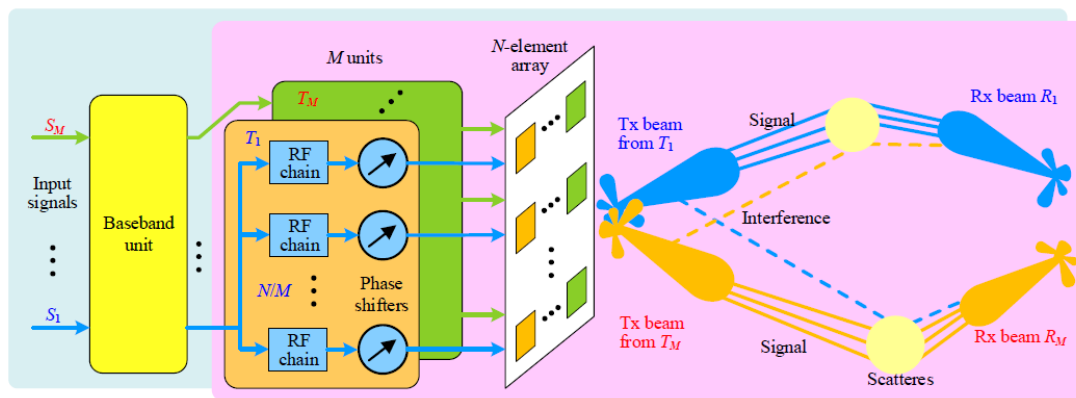
1. Y. Yu, H. Liu, Y. Wu, and K. Kang, "A 54.4–90 GHz low-noise amplifier in 65-nm CMOS,"IEEE J. Solid-State Circuits, vol. 52, no. 11,pp. 2892–2904, Nov. 2017
2. B.-J. Huang, K.-Y. Lin, and H. Wang, "Millimeter-wave low power andminiature CMOS multicascode low-noise amplifiers with noise reduc-tion topology,"IEEE Trans. Microw. Theory Techn., vol. 57, no. 12,pp. 3049–3059, Dec. 2009.
3. Ramzan, "A 1.4V 25mW Inductorless Wideband LNA in 0.13μm CMOS",DOI: 10.1109/ISSCC.2007.373475, IEEE International Solid State Circuits Conference (ISSCC), , California, USA, 11-15 Feb, 2007.
4. S. Onoe, "Evolution of 5G mobile technology toward 2020 and beyond,"inProc. IEEE Int. Solid-State Circuits Conf. (ISSCC), San Francisco,CA, USA, 2016, pp. 23–28.

### Project-4: mm Wave Phase Shifter for MMIMO Application

Millimeter-wave (mmWave) systems avail of extremely large bandwidth and can therefore boost peak data rates and improve user experience. The adoption of beamforming in mmWave systems, for the purpose of compensating the severe path loss and improving the effective signal-to-interference-plus-noise ratio (SINR), necessitates the use of MMIMO systems. As crucial components in any large-scale phased antenna array, phase shifters have attracted considerable interest recently. Generally, there are two basic types of phase shifters for mmWave systems: active phase shifters and passive phase shifters. By making efficient use of active modules, the former outperform their passive counterparts in terms of insertion loss and maximize the spectral efficiency.

All the existing phase shifter topologies do not meet the requirement of the small chip area, low phase error, large tuning range, and insertion loss at same time. This is new area and there is large room for innovative designs and new ideas.

The minimum phase shifter resolution is determined by the directivity of the array. At each beamforming angle, the phase setting of each element is chosen such that the total array gain is maximized at that angle, 4-bit might be enough for any array size from the perspective of array gain. However, higher phase shifter resolution reduces the maximum side lobe and increases the minimum peak-to-null ratio, which is highly desired to minimize interference and multi-path fading.



**Skill Development:** Analog and RF Circuit Design, mm-Wave Circuits, Signal Integrity, CMOS transistor modeling, Extreme Layout Optimization, Impedance Matching, Amplification at mm-Wave

**Innovation Aspects:** ★★★★★ (4.5/5)

**Research Areas:** DSP, 5G/6G Transceivers, Phase Array Radars, Future MIMO and MMIMO System

**Application Areas:** 5G/6G Transceivers, Phase Array Radars, Base Stations, Future Satellite Transceivers

#### References:

1. L. C. Godara, "The Effect of Phase-Shifter Errors on the Performance of an Antenna-Array Beamformer," IEEE J. Oceanic Eng., vol. OE-10, July 1985, pp. 278–84,
2. S. Onoe, "Evolution of 5G mobile technology toward 2020 and beyond," in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), San Francisco, CA, USA, 2016, pp. 23–28.

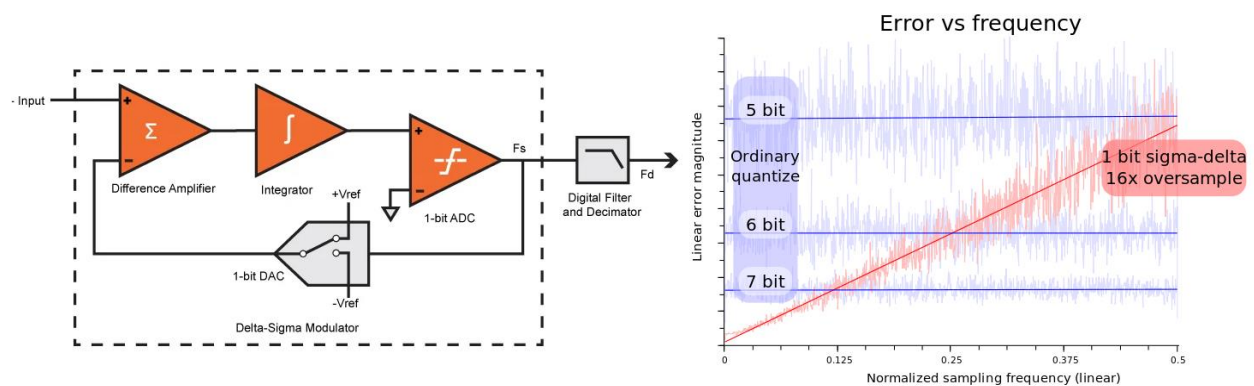
"Advanced Architectures for efficient mm-Wave transmitters" PHD Thesis by Jiashu Chen, 2013.



### Project-5: Massive MIMO Channel Estimation with Low-Resolution Spatial Sigma-Delta ADC

In massive MIMO implementations operating with high bandwidths, as in a millimeter wave application; a 100-element antenna array sampled at 500 Msamples/sec with a 10-bit ADC requires a 1Tb/sec data pipeline from the RRH to the baseband processor. One-bit sampling can significantly alleviate this requirement. While it has been shown that one-bit quantization a small degradation at low SNRs and offers significant ad-vantages in terms of power consumption and implementation complexity, at medium to high SNRs the performance loss is substantial. The concept of  $\Sigma\Delta$  modulation can also be applied in the spatial as well as the temporal domain.

In this project we will design a  $\Sigma\Delta$  ADC which is suitable for the Massive MIMO Channel Estimation employed in 5G and 6G future systems.



**Skill Development:** Z Transform, Noise Shaping, Verilog Coding, Analog and RF Design, FPGA Decimation Block outside the chip, GHz Interfaces.

**Innovation Aspects:** ★★★★★ (4/5)

**Application Areas:** ADC Converters, 5G/6G systems, Low Power Transceivers, High Resolution Digitization, Medical Imaging, High Resolution Audio Recording.

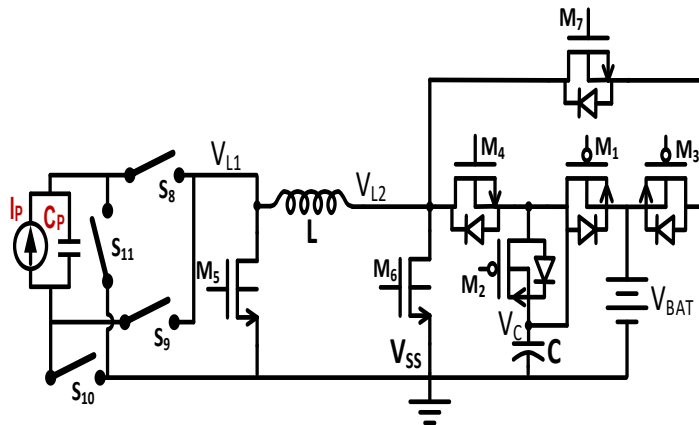
#### References:

1. G. C. Temes and J. C. Candy, "A tutorial discussion of the oversampling method for A/D and D/A conversion," IEEE International Symposium on Circuits and Systems, New Orleans, LA, USA, 1990, pp. 910-913 vol.2, doi: 10.1109/ISCAS.1990.112241.
2. Rao, G. Seco-Granados, H. Pirzadeh, and A. L. Swindlehurst. "Massive MIMO Channel Estimation with Low-Resolution Spatial Sigma-Delta ADCs". [Online]. Available: <https://arxiv.org/abs/2005.0775>, (May 15, 2020)
3. M. Shao, W. Ma, Q. Li and L. Swindlehurst, "Spatial Sigma-Delta Modulation for the Massive MIMO Downlink," 2019 53rd Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, CA, USA, 2019, pp. 833-837, doi: 10.1109/IEEECONF44664.2019.9048918.



### Project-6: Capacitor-less High Efficiency Triboelectric Energy Harvester

Since the development of first triboelectric nano generator (TENG) in 2012, it has gained quite an attention due to its high energy density property. However, all of the implemented TENG harvesting circuits have a capacitor at the rectified TENG output, which reduces TENG source energy by added load/capacitor. However, the energy extraction from TENG can be maximized by isolating load from TENG source charging, followed by charge transfer from TENG to battery at each voltage peaking event. This approach necessitates load isolation harvesting topology for efficient harvesting from TENG, In this work, we have plan to design a TENG biasing, and load isolation harvesting topology, to maximize the energy density of TENG harvesting system.



**Skill Development:** Power Management Unit, Multi-Voltage level interfacing schemes, IC Interface design, Comparator design, Layout Optimization.

**Innovation Aspects:** ★★★★★★★★

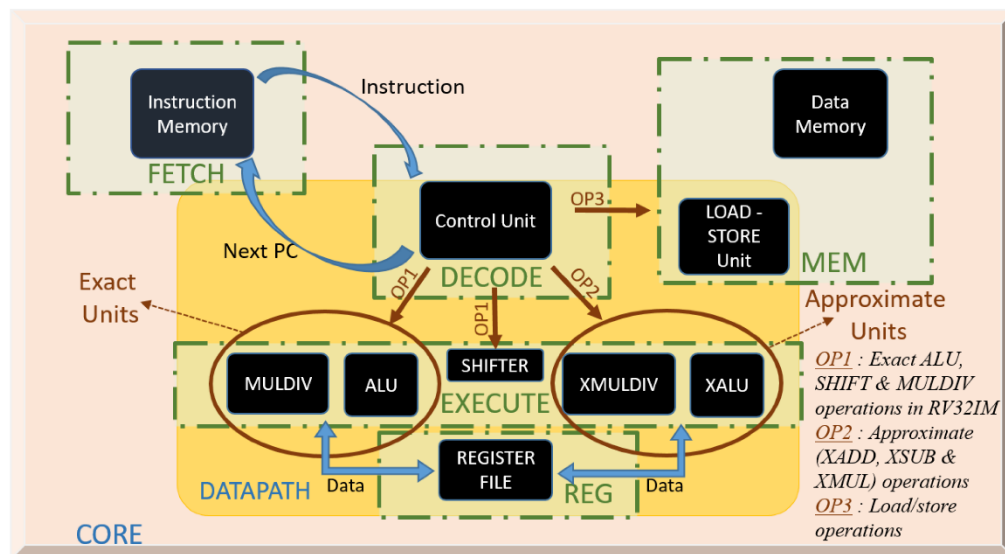
**Application Areas:** Nano generators, Energy Harvester, Power Management, Inductor based-TENG Harvesting

#### References:

4. K. Rawy, R. Sharma, H. J. Yoon, et al., "An 88% Efficiency 2.4 $\mu$ W to 15.6 $\mu$ W Triboelectric Nanogenerator Energy Harvesting System Based on a Single-Comparator Control Algorithm", IEEE Asian Solid-State Circuits Conference (A-SSCC), Taiwan, 5-7 Nov. 2018
5. I. Park, et al., "A 4.5-to-16 $\mu$ W integrated triboelectric energy-harvesting system based on high-voltage dual-input buck converter with MPPT and 70V maximum input voltage", IEEE International Solid State Circuits Conference (ISSCC), California, USA, Feb, 2018.
6. Wang S, Xie Y, Niu S, et al., "Maximum surface charge density for triboelectric nanogenerators achieved by ionized-air injection: methodology and theoretical understanding", Advanced Materials (Deerfield Beach, Fla.). 2014 Oct;26(39):6720-6728. DOI: 10.1002/adma.201402491.
7. W. Liu, Z. Wang, G. Wang, G. Liu, et al., "Integrated charge excitation triboelectric nanogenerator", Nat Commun 10, 1426 (2019).

### Project-7: ASIC Implementation of ALU based on Approximate Computing Techniques

In modern embedded designs, strict power constraints and quest of high performance require new design strategies to be evolved. One such emerging design methodology is named as approximate computing. A variety of applications related with computer vision, data mining, image/video processing and deep learning neural networks, etc. can be error-tolerant in some cases. Therefore, approximate computing paradigm produce less accurate but acceptable quality results by relaxing the stringent error requirement. Arithmetic units are normally the basic building blocks and are an integral part of the computing hardware designs and consume considerable amount of processing time and power. Therefore, approximation in arithmetic unit's hardware can be very beneficial. In this project, approximate computing based arithmetic units (adders or multipliers) will be studied and implemented in ASIC, while incorporating optimizations that come with ASIC design methodologies.



**Skill Development:** RTL coding in Verilog, FPGA Prototyping, Digital ASIC Design and Development in 65nm CMOS

**Application Areas:** Comparison of power and logic between FPGA and ASIC implementations. Optimization during the process of mapping the design for ASIC standard cell libraries. Low Power Computing, Efficient Computing,

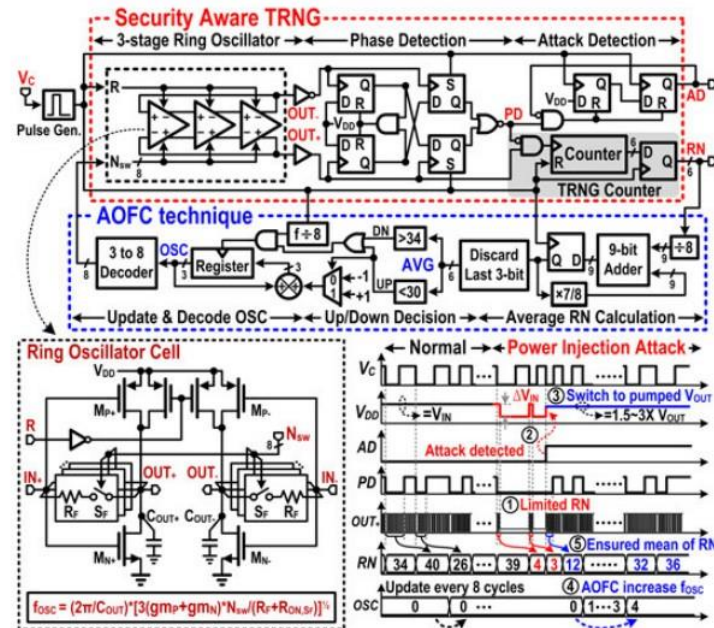
**Innovation Aspects:** ★★★★★ (3/5)

#### References:

1. Ramasamy, Manickam & Ganesamoorthy, Narmadha & Deivasigamani (2019). Carry based approximate full adder for low power approximate computing. 10.1109/ICSCC.2019.8843644.
2. N. Huang, S. Chen and K. Wu, "Sensor-Based Approximate Adder Design for Accelerating Error-Tolerant and Deep-Learning Applications," 2019 Design, Automation & Test in Europe Conference & Exhibition (DATE), Florence, Italy, 2019, pp. 692-697.
3. Esposito, Darjn & Strollo, Antonio & Napoli, E. & De Caro, Davide & Petra, Nicola. (2018). Approximate Multipliers Based on New Approximate Compressors. IEEE Transactions on Circuits and Systems I: Regular Papers. PP. 1-14. 10.1109/TCSI.2018.2839266.

### Project-8: Oscillator based True Random Number Generator for 5G NR Applications

Cryptographic key generator is an essential component of an encryption system. State-of-the-art suggest use of Ring Oscillators and PUFs to develop a true random number generator and cryptographic key generator. Some modifications in the existing work could make the designs attack resilient and add the aspect of novelty. In this project we will design and implement the TRNG generator block for 5G NR on-chip applications.



**Skill Development:** Cryptographic Circuit development, Analog Cell Design, Digital Cell Design, ASIC development

**Innovation Aspects:** ★★★★★ (4/5)

**Application Areas:** Cryptographic Chips, Secure Processor, The secure key in 5G NR, Encrypted Transmission

#### References:

1. Li, TangShengSheng, et al. "A novel transition effect ring oscillator based true random number generator for a security SoC." *2017 International Conference on Electron Devices and Solid-State Circuits (EDSSC)*. IEEE, 2017.
2. Liu, Dongsheng, et al. "A low-cost low-power ring oscillator-based truly random number generator for encryption on smart cards." *IEEE Transactions on Circuits and Systems II: Express Briefs* 63.6 (2016): 608-612.
3. Buchovecka, Simona, et al. "True random number generator based on ring oscillator PUF circuit." *Microprocessors and Microsystems* 53 (2017): 33-41.
4. Maes, Roel, et al. "Secure key generation from biased PUFs: extended version." *Journal of Cryptographic Engineering* 6.2 (2016): 121-137.